FS8600

Fail-safe system basis chip with multiple SMPSs and LDOs

Rev. 2 — 2 December 2022 Product data sheet
CONFIDENTIAL

1 General description

The FS86 device family, SW compatible with FS84/85 family, expands the power capability, the safety integration and system scalability of domain controller applications to address the multiple MCU requirements present in ADAS, radar and electrification applications.

The FS86 includes multiple switch mode and linear voltage regulators, and enhanced safety features with Fail-Safe outputs. The latest NXP HV Buck architecture features a 15 A capability with e-fuse protection to shut down the system power to prevent any damage in case of a harmful event. The ability to monitor ten voltages with +/-1% accuracy extends the system safety concept by allowing QM rails from others components to be monitored.

With its innovative synchronization feature, the FS86 is part of the BYLink System Power Platform, enabling a new smart approach to designing Safe System Power Management. It provides power, safety and system scalability to ease platform development strategies. Cascaded system SBC/PMICs behave as ONE with safety and sequencing synchronization.

The FS86 is part of a complete family of devices that offer scalability in power and safety, and provide pin-to-pin and software compatibility. It is developed in compliance with the ISO 26262 standard and is qualified according to AEC-Q100 requirements.

2 Features and benefits

Operating Range

- 60 V DC maximum input voltage for 24 V battery network applications
- 36 V DC maximum input voltage for 12 V battery network applications
- Support operating voltage range down to 4.5 V battery voltage with V_{PRE} = 3.3 V
- Low Power OFF mode with low sleep current (10 µA typ.)

Power Supplies

- VPRE: Synchronous high voltage buck controller with external FETs
  - Configurable output voltage from 3.3 V to 5.0 V and current capability up to 15 A DC
  - Selectable switching frequency in force PWM with APS
- BOOST: Low voltage boost converter with integrated low-side FET
  - Configurable output voltage from 5 V to 6 V and current capability up to 1 A DC
- BUCK: Low voltage integrated synchronous BUCK converter
  - Configurable output voltage from 1.0 V to 3.3 V and current capability up to 2.5 A DC
- LDO1: Low voltage LDO regulator for MCU I/O and system peripheral support with load switch capability
  - Configurable output voltage from 1.5 V to 5.0 V and current capability up to 400 mA DC
- LDO2: Medium voltage LDO regulator for MCU I/O and system peripheral support
  - Configurable output voltage from 1.1 V to 5.0 V and current capability up to 400 mA DC

System support

- 2x input pins for wake-up detection, 3.3 V compatible and battery voltage sensing capability
- Analog Multiplexer with full System Voltages monitoring
- Enhanced leader/follower power up sequencing management thru XFAILB pin
- 10 ms optional RSTB release delay during power up for certain MCU compliancy
- Device control via 32 bits I2C interface with 8-bit CRC

Compliancy

- EMC optimization features on switching regulators including spread spectrum, slew rate control and manual frequency tuning
- EMI robustness supporting various automotive EMI Test standards
- Conducted Emission: IEC 61967-4
- Conducted Immunity: IEC 62132-4
- Radiated emission: FMC1278 rev. 3 from 2018
- Radiated immunity: FMC1278 from 2018 and ISO11452-4

Functional Safety

- Scalable portfolio to fit for ASIL B to ASIL D Automotive Safety Systems
- Independent voltage Monitoring Circuitry
- Up to 10 voltage monitoring input for FS86 and external PMIC voltage rails with 1 % target accuracy
- Dedicated interface for MCU monitoring with simple or challenger watchdog monitoring
- MCU hardware failure monitoring with PWM monitoring capability (FCCU)
- External IC failure monitoring (ERRMON)

- Logical and Analog Built-in Self-Test (LBIST, ABIST)
- Safety Outputs with latent fault detection mechanism (PGOOD, RSTB, FS0B)

Configuration and Enablement

- QFN 48 pins with exposed pad for optimized thermal management
- OTP programming for device customization

3 Applications

- Domain controller (ADAS, electrification, Infotainment, etc.)
- Radar (radar, imaging radar)
- Vision (mono camera, stereo camera, night vision, etc.)
- 24 V battery network (60 V maximum): Truck, bus, transportation
- 12 V battery network (36 V maximum): Automotive

4 Simplified Application Diagram

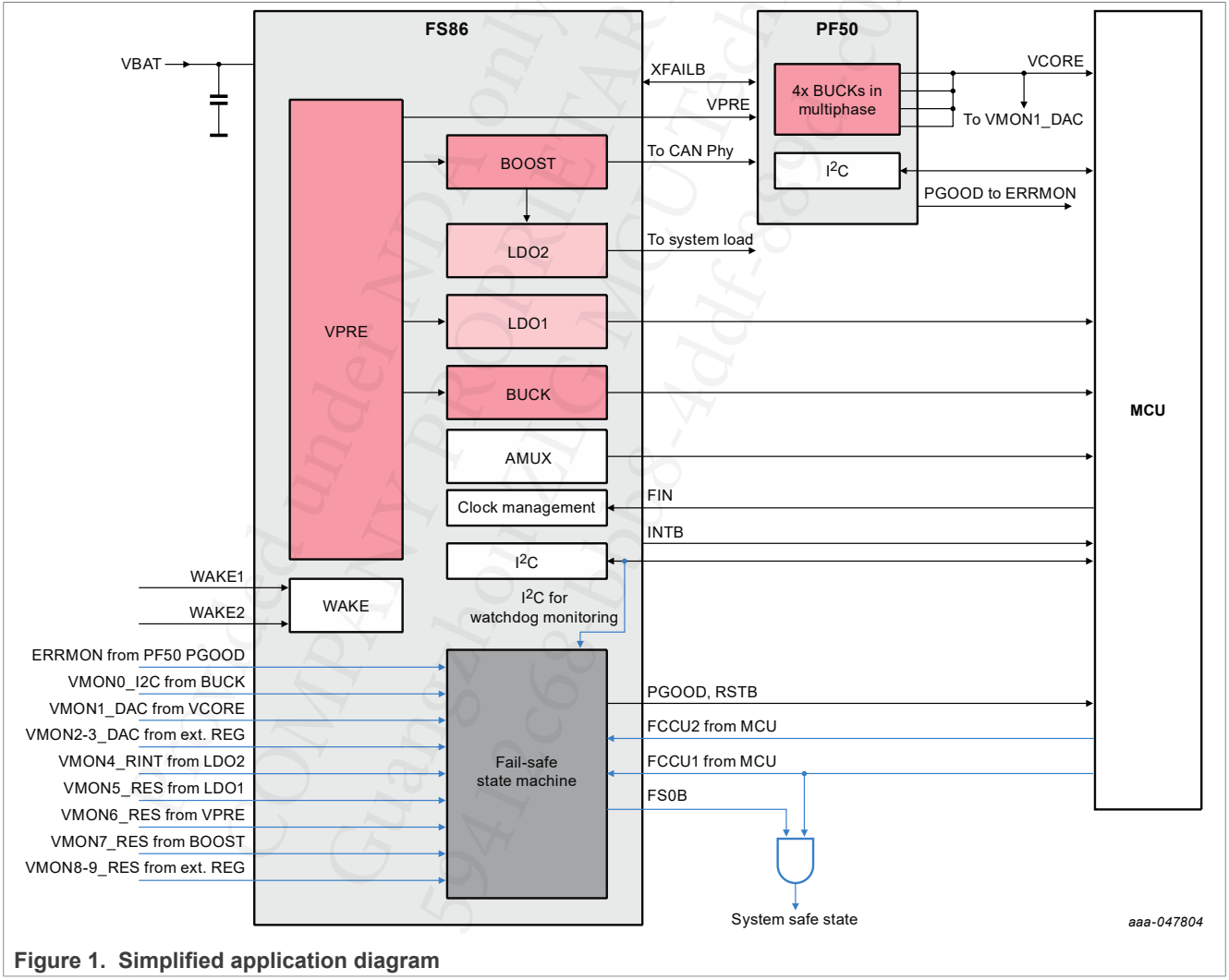


Figure 1. Simplified application diagram

5 Ordering information

5.1 Device family

FS8600 device family (called FS86 hereafter) provides selectable features based on part numbering and OTP configuration.

Table 1. Device options

FS + Core ID	Application	VSUP max rating	VPRE	BOOST	BUCK	LDOs	VMONs	Watchdog	FCCU	ERRMON	FIN
FS8600	24 V battery network	60 V	Yes	Yes	No	2	4[1]	Yes[2]	Yes	Yes	Yes
FS8601		60 V	Yes	Yes	No	2	6[1]		Yes	Yes	Yes
FS8602		60 V	Yes	Yes	No	2	8[1]		Yes	Yes	Yes
FS8603		60 V	Yes	Yes	No	2	10[1]		Yes	Yes	No[3]
FS8610		60 V	Yes	Yes	Yes	2	4[1]		Yes	Yes	Yes
FS8611		60 V	Yes	Yes	Yes	2	6[1]		Yes	Yes	Yes
FS8612		60 V	Yes	Yes	Yes	2	8[1]		Yes	Yes	Yes
FS8613		60 V	Yes	Yes	Yes	2	10[1]		Yes	Yes	No[3]
FS8620	12 V battery network	36 V	Yes	Yes	No	2	4[1]		Yes	Yes	Yes
FS8621		36 V	Yes	Yes	No	2	6[1]		Yes	Yes	Yes
FS8622		36 V	Yes	Yes	No	2	8[1]		Yes	Yes	Yes
FS8623		36 V	Yes	Yes	No	2	10[1]		Yes	Yes	No[3]
FS8630		36 V	Yes	Yes	Yes	2	4[1]		Yes	Yes	Yes
FS8631		36 V	Yes	Yes	Yes	2	6[1]		Yes	Yes	Yes
FS8632		36 V	Yes	Yes	Yes	2	8[1]		Yes	Yes	Yes
FS8633		36 V	Yes	Yes	Yes	2	10[1]		Yes	Yes	No[3]

[1] Maximum number allowed. Any VMONx can be enabled up to this limit.
[2] ASIL B: Watchdog Simple. ASIL D: Watchdog Challenger.
[3] FIN and VMON9 cannot be used at the same time (same pin)

5.2 Part numbering

M	FS	8600	B	M	B	A0	ES
P: prototype M: standard S: custom	HV PMIC	FS86 Core ID[1]	Silicon revision A: A0 B: A1	Ambient temperature (T_A) M: –40 °C to 125 °C	ASIL B: ASIL B D: ASIL D	OTP code A0: OTP A0 xx: OTP xx	Package type ES: dimple wettable flank

[1] See Table 1

Table 2. Ordering information

Part Number[1]	Application	ASIL	Package		
			Name	Description	Version
MFS8600BMBA0ES[2]	24 V battery network	B	HPQFN48eP	HPQFN48, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT619-26
MFS8601BMBA0ES[2]					
MFS8602BMBA0ES[2]					
MFS8603BMBA0ES[2]					

Table 2. Ordering information*...continued*

Part Number[1]	Application	ASIL	Package		
			Name	Description	Version
MFS8610BMBA0ES[2]					
MFS8611BMBA0ES[2]					
MFS8612BMBA0ES[2]					
MFS8613BMBA0ES[2]					
MFS8600BMDA0ES[2]					
MFS8601BMDA0ES[2]					
MFS8602BMDA0ES[2]					
MFS8603BMDA0ES[2]		D			
MFS8610BMDA0ES[2]					
MFS8611BMDA0ES[2]					
MFS8612BMDA0ES[2]					
MFS8613BMDA0ES[2]					
MFS8620BMBA0ES[2]					
MFS8621BMBA0ES[2]					
MFS8622BMBA0ES[2]					
MFS8623BMBA0ES[2]					
MFS8630BMBA0ES[2]		B			
MFS8631BMBA0ES[2]					
MFS8632BMBA0ES[2]					
MFS8633BMBA0ES[2]	12 V battery network				
MFS8620BMDA0ES[2]					
MFS8621BMDA0ES [2]					
MFS8622BMDA0ES[2]					
MFS8623BMDA0ES[2]					
MFS8630BMDA0ES[2]		D			
MFS8631BMDA0ES[2]					
MFS8632BMDA0ES[2]					
MFS8633BMDA0ES[2]					
PFS8613AMDA0ES[3]	12 V or 24 V battery network	B or D			
PFS8613BMDA0ES[4]					

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Production part number available only after product qualification (A1 silicon pass).
[3] Superset part number that can cover all features for prototype ordering (A0 silicon pass/obsolete)..
[4] Superset part number that can cover all features for prototype ordering (A1 silicon pass).

Part numbers ending with A0 OTP code are non-programmed OTP configuration. Pre-programmed OTP configurations are managed through part number extension. For a custom OTP configuration, please contact your local NXP sales representative.

6 Internal block diagram

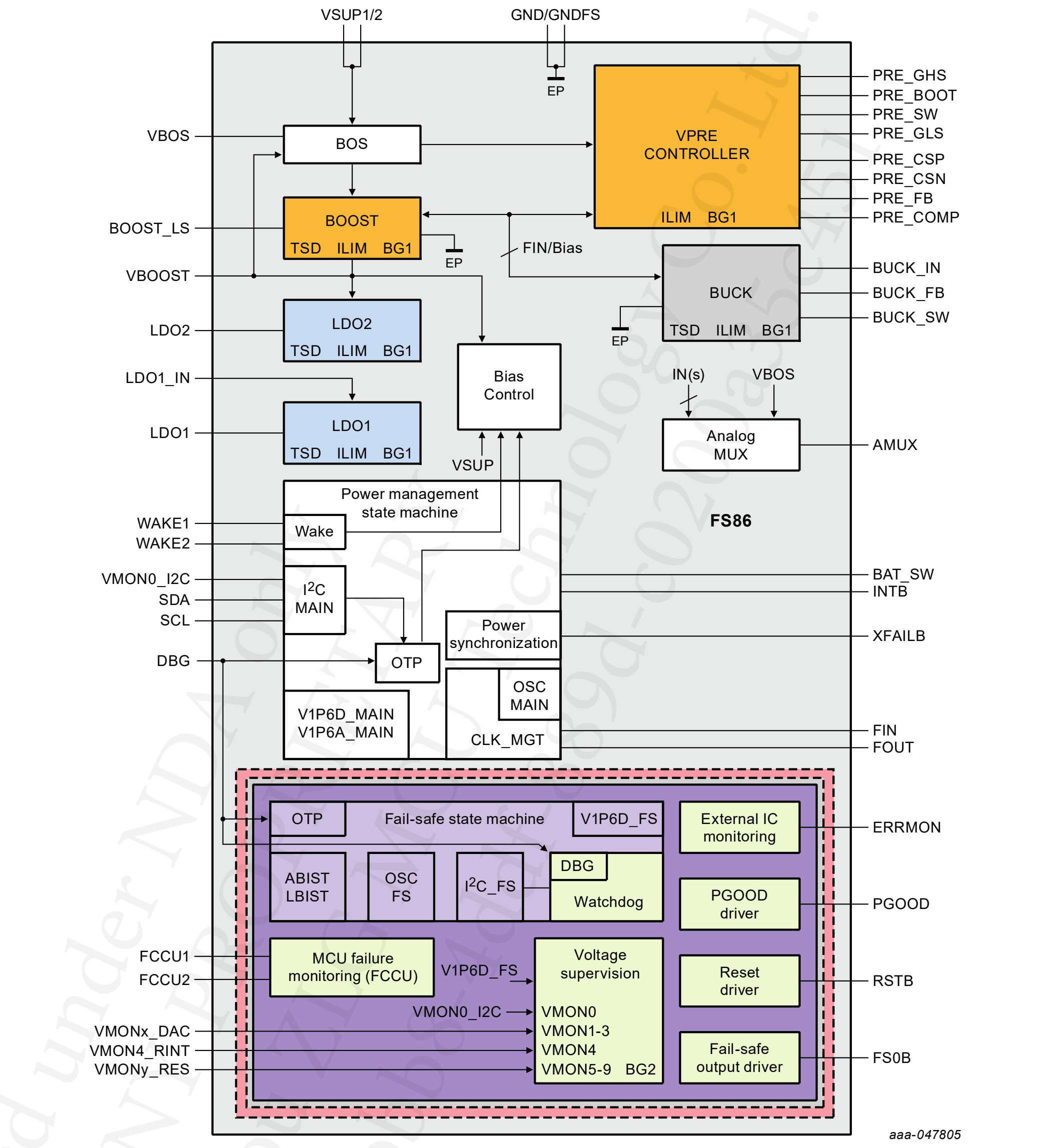


Figure 2. Block diagram

7 Pinout information

7.1 Pinout

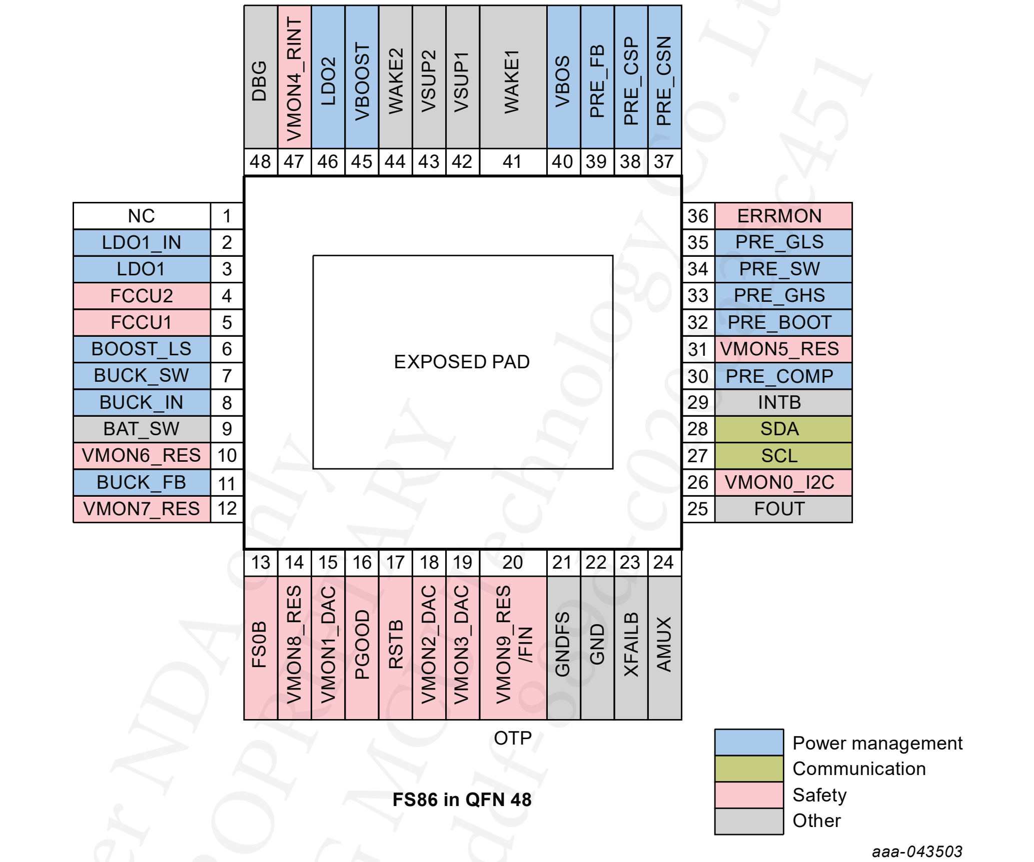


Figure 3. Pin configuration

7.2 Pin description

Table 3. Pin description

Pin	Name	Type	Description
1	N/C	N/C	Not connected pin
2	LDO1_IN	Analog input	Linear regulator #1 input voltage
3	LDO1	Analog output	Linear regulator #1 output voltage
4	FCCU2	Digital input	MCU Error Monitoring input 2
5	FCCU1	Digital input	MCU Error Monitoring input 1
6	BOOST_LS	Analog input	BOOST Low Side Drain of internal MOSFET
7	BUCK_SW	Analog output	Low Voltage Buck switching node
8	BUCK_IN	Analog input	Low Voltage Buck input voltage
9	BAT_SW	Digital output	Battery switch control output. Active Low. Open drain structure.
10	VMON6_RES	Analog input	External resistor bridge voltage monitoring input #6

Table 3. Pin description*...continued*

Pin	Name	Type	Description
11	BUCK_FB	Analog input	Low Voltage Buck voltage feedback.
12	VMON7_RES	Analog input	External resistor bridge voltage monitoring input #7
13	FS0B	Digital output	Fail Safe Output 0. Active Low. Open drain structure.
14	VMON8_RES	Analog input	External resistor bridge voltage monitoring input #8
15	VMON1_DAC	Analog input	DAC voltage monitoring input #1
16	PGOOD	Digital output	Power good output
17	RSTB	Digital input/output	Reset output. Active Low. The main function is to reset the MCU. Reset input voltage is monitored in order to detected external reset and fault condition
18	VMON2_DAC	Analog input	DAC voltage monitoring input #2
19	VMON3_DAC	Analog input	DAC voltage monitoring input #3
20	VMON9_RES	Analog input	External resistor bridge voltage monitoring input #9. Exclusive with FIN (OTP)
20	FIN	Digital input	Frequency synchronization input. Exclusive with VMON9_RES (OTP)
21	GNDFS	Ground	Fail Safe ground
22	GND	Ground	Main ground
23	XFAILB	Digital input/output	Power Synchronization input/output with NXP low voltage PMIC
24	AMUX	Analog output	Multiplexed output to be connected to an MCU ADC with selection of the analog parameter thru I2C.
25	FOUT	Digital output	Frequency synchronization output or digital output (OTP)
26	VMON0_I2C	Analog input	Input voltage for FIN, AMUX, I2C, INTB, FCCU, ERRMON. Internal resistor bridge voltage monitoring input #0
27	SCL	Digital input	I2C Bus. Clock input
28	SDA	Digital input/output	I2C Bus. Bidirectional data line
29	INTB	Digital output	Interrupt output
30	PRE_COMP	Analog input	VPRE compensation network and negative current sense input
31	VMON5_RES	Analog input	External resistor bridge voltage monitoring input #5
32	PRE_BOOT	Analog input/output	VPRE bootstrap capacitor
33	PRE_GHS	Analog output	VPRE High Side gate driver for external MOSFET
34	PRE_SW	Analog output	VPRE switching node
35	PRE_GLS	Analog output	VPRE Low Side gate driver for external MOSFET
36	ERRMON	Digital input	External IC error monitoring input
37	PRE_CSN	Analog input	VPRE negative current sense input
38	PRE_CSP	Analog input	VPRE positive current sense input
39	PRE_FB	Analog input	VPRE voltage feedback.
40	VBOS	Analog output	Best of supply output voltage
41	WAKE1	Digital/Analog input	Wake up input 1 (thru ext. serial resistor)

Table 3. Pin description*...continued*

Pin	Name	Type	Description
42	VSUP1	Power Analog Input	Power supply of the device #1. An external reverse battery protection diode in series is mandatory
43	VSUP2	Power Analog Input	Power supply of the device #2. An external reverse battery protection diode in series is mandatory
44	WAKE2	Digital/Analog input	Wake up input 2 (thru ext. serial resistor)
45	VBOOST	Analog output	Boost output voltage
46	LDO2	Analog output	Linear regulator #2 output voltage
47	VMON4_RINT	Analog input	Internal resistor bridge voltage monitoring input #4
48	DBG	Analog input	DEBUG Mode entry and OTP input supply
EP	EP	Ground	Expose pad must be connected to GND

8 Connection of unused pins

Table 4. Connection of unused pins

Pin	Name	Type	Description
1	N/C	N/C	Open
2	LDO1_IN	Analog input	Open – power sequence slot 15, OTP LDO1S[3:0] = '1111'
3	LDO1	Analog output	Open
4	FCCU2	Digital input	Open – 200 kΩ internal pull up to VMON0_I2C
5	FCCU1	Digital input	Open – 800 kΩ internal pull down to GND
6	BOOST_LS	Analog input	See Section 24.5 "BOOST not populated"
7	BUCK_SW	Analog output	Open
8	BUCK_IN	Analog input	Open
9	BAT_SW	Digital output	Open
10	VMON6_RES	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON6_EN = 0
11	BUCK_FB	Analog input	Open – 1.5 MΩ Internal resistor bridge pull down to GND
12	VMON7_RES	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON7_EN = 0
13	FS0B	Digital output	Open – 2 MΩ internal pull down to GND
14	VMON8_RES	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON8_EN = 0
15	VMON1_DAC	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON1_EN = 0
16	PGOOD	Digital output	Connection mandatory
17	RSTB	Digital output	Connection mandatory
18	VMON2_DAC	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON2_EN = 0
19	VMON3_DAC	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON3_EN = 0
20	VMON9_RES	Analog input	Open
20	FIN	Digital input	Open
21	GNDFS	Ground	Connection mandatory

Table 4. Connection of unused pins*...continued*

Pin	Name	Type	Description
22	GND	Ground	Connection mandatory
23	XFAILB	Digital input/output	Connection to GND
24	AMUX	Analog output	Open
25	FOUT	Digital output	Open – push pull structure
26	VMON0_I2C	Analog input	Connection mandatory
27	SCL	Digital input	External pull down to GND
28	SDA	Digital input/output	External pull down to GND
29	INTB	Digital output	Open – 10 kΩ internal pull up to VMON0_I2C
30	PRE_COMP	Analog input	See Section 22.11 "VPRE not populated"
31	VMON5_RES	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON5_EN = 0
32	PRE_BOOT	Analog input/output	See Section 22.11 "VPRE not populated"
33	PRE_GHS	Analog output	See Section 22.11 "VPRE not populated"
34	PRE_SW	Analog output	See Section 22.11 "VPRE not populated"
35	PRE_GLS	Analog output	See Section 22.11 "VPRE not populated"
36	ERRMON	Digital input	External pull down to GND
37	PRE_CSN	Analog input	See Section 22.11 "VPRE not populated"
38	PRE_CSP	Analog input	See Section 22.11 "VPRE not populated"
39	PRE_FB	Analog input	Connection mandatory. See Section 22.11 "VPRE not populated"
40	VBOS	Analog output	Connection mandatory
41	WAKE1	Digital/Analog input	External pull down to GND
42	VSUP1	Power Analog Input	Connection mandatory
43	VSUP2	Power Analog Input	Connection mandatory
44	WAKE2	Digital/Analog input	External pull down to GND
45	VBOOST	Analog output	Connection mandatory. See Section 24.5 "BOOST not populated"
46	LDO2	Analog output	Open – power sequence slot 15, OTP LDO2S[3:0] = '1111'
47	VMON4_RINT	Analog input	Open – 2 MΩ internal pull down to GND, OTP VMON4_EN = 0
48	DBG	Analog input	External pull down to GND
EP	EP	Ground	Connection mandatory

9 Maximum ratings

Table 5. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Conditions	Parameter	Min	Max	Unit
Voltage ratings of 24 V network application part numbers (see Table 2)					
VSUP1/2	DC Voltage	VSUP1,2 pins	−0.3	60	V
WAKE1/2	DC Voltage	WAKE1,2 pins (external series resistor mandatory)	−1.0	60	V
FS0B	DC Voltage	FS0B pin	−0.3	60	V
BAT_SW	DC Voltage	BAT_SW pin	−0.3	60	V
PRE_SW	DC Voltage	PRE_SW pin	−2.0	60	V
	Transient voltage < 20 ns		−3.0	60	
PRE_GHS, PRE_BOOT	DC Voltage	PRE_GHS, PRE_BOOT pins	−0.3	65.5	V
Voltage ratings of 12 V network application part numbers (see Table 2)					
VSUP1/2	DC Voltage	VSUP1,2 pins	−0.3	36	V
WAKE1/2	DC Voltage	WAKE1,2 pins (external series resistor mandatory)	−1.0	36	V
FS0B	DC Voltage	FS0B pin	−0.3	36	V
BAT_SW	DC Voltage	BAT_SW pin	−0.3	36	V
PRE_SW	DC Voltage	PRE_SW pin	−2.0	36	V
	Transient voltage < 20 ns		−3.0	36	
PRE_GHS, PRE_BOOT	DC Voltage	PRE_GHS, PRE_BOOT pins	−0.3	41.5	V
Voltage ratings of general pins					
BOOST_LS	DC Voltage	BOOST_LS pin	−0.3	8.5	V
VBOOST	DC Voltage	VBOOST pin	−0.3	6.5	V
BUCK_IN	DC Voltage	BUCK_IN pin	−1.0	5.5	V
	Transient voltage < 3 µs		−1.0	6.5	
BUCK_SW	Transient voltage < 20 ns	BUCK_SW pin	−0.3	6.5	V
VMONx	DC Voltage	VMONx_DAC 1-3, VMONy_RES 5-9	−0.3	36	V
DBG	DC Voltage	DBG pin	−0.3	10	V
All other pins	DC Voltage	at all other pins	−0.3	5.5	V

10 Electrostatic discharge

10.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model standard with 100 pF and 1.5 kΩ. This protection is ensured at all pins.

10.2 Charged device model

The device is protected up to ±750 V on corner pins and up to ±500 V on all other pins, according to the AEC Q100 - 011 charged device model standard.

10.3 Discharged contact test

The device is protected up to ±8 kV, according to the following discharged contact tests.

- Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
- Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
- Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2, FS0B pins.

11 Operating range

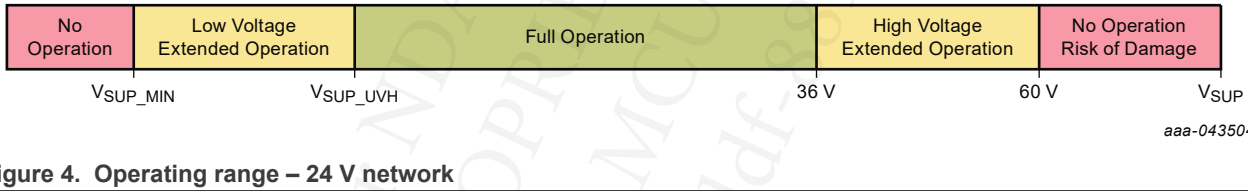


Figure 4. Operating range – 24 V network

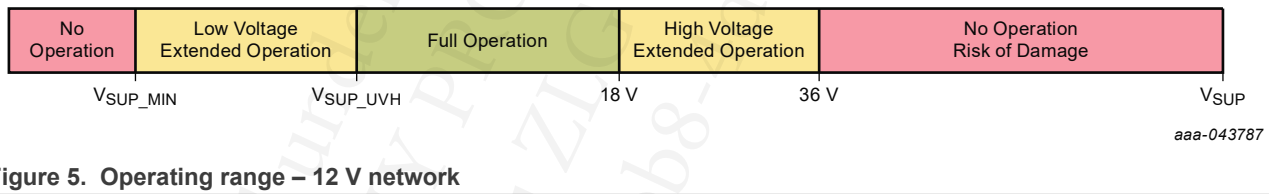


Figure 5. Operating range – 12 V network

Figure 4 and Figure 5 legend:

- No Operation: device is not providing the expected functionality or is shut down.
- Low Voltage Extended Operation: device remains functional but with reduced electrical performance.
  - VPRE may be in drop out mode. VPRE output voltage may decrease below its nominal value and the transient load will be degraded.
- Full Operation: device is providing the expected functionality with full electrical performance within the limits of the datasheet and within the operating mission profile of the safety manual.
- High Voltage Extended Operation: device is providing the expected functionality with full electrical performance within the limits of the datasheet but for a limited period of time.
  - This could occur during load dump or double-battery jump start events for example.
- Risk of Damage: device is overstressed with a risk of damaging the device.

Operating range example

Assumptions:

- L_{PI_DCR} = 20 mΩ
- BAT_SW PMOS R_{DSon} = 20 mΩ
- PRE HS/LS MOS R_{DSon} = 20 mΩ
- L_{PRE_DCR} = 20 mΩ
- PRE R_{SHUNT} = 20 mΩ
- D_{MAX} = 96 % with F_{PRE_SW} = 455 kHz and $T_{PRE\_OFF\_MIN}$ = 80 ns
- I_{PRE} = 3.0 A
- V_{RBD} = 0.56 V
- $V_{SUP\_MIN} \approx (L_{PI\_DCR}$ + BAT_SW PMOS R_{DSon} + PRE HS/LS MOS R_{DSon} + L_{PRE_DCR} + PRE $R_{SHUNT}) \times I_{PRE} + V_{PRE\_UVL} / D_{MAX}$
- $V_{BAT\_MIN} \approx V_{SUP\_MIN} + V_{RBD}$
- $V_{SUP\_MIN} \approx$ 3.1 V when $V_{PRE} = V_{PRE\_UVL}$
- $V_{BAT\_MIN} \approx$ 3.7 V when $V_{PRE} = V_{PRE\_UVL}$

Operating range

- Below V_{SUP_UVH} threshold, the extended operation range depends on VPRE output voltage configuration and external components.
  - When VPRE is configured at 5.0 V, V_{PRE} may not remain in its regulation range;
  - VSUP minimum voltage depends on external components (L_{PI_DCR}, L_{PRE_DCR}, BAT_SW PMOS R_{DSon}, PRE HS R_{DSon}) and application conditions (I_{PRE}, F_{PRE_SW}).
- When VPRE switching frequency F_{PRE_SW} is 455 kHz, the FS86 maximum continuous operating voltage is 36 V. It has been validated at 48 V for limited duration of 1 hour at room temperature to satisfy the jump start requirement of 24 V applications. It can sustain 58 V load dump without external protection. Note that some part numbers are not adapted for 24 V continuous operation.
- When VPRE switching frequency F_{PRE_SW} is 2.22 MHz, the FS86 maximum continuous operating voltage is 18 V. It has been validated at 28 V for limited duration of 2 minutes at room temperature to satisfy the jump start requirement of 12 V applications and 35 V load dump.

12 Thermal ratings

Table 6. Thermal ratings

Symbol	Description (Rating)	Min	Max	Unit
Thermal ratings				
T_A	Ambient Temperature (Grade 1)	−40	125	°C
T_J	Junction Temperature (Grade 1)	−40	150	°C
T_{STG}	Storage Temperature	−55	150	°C
Thermal resistance (per JEDEC JESD51-2 and JESD51-8)				
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (2s2p)	—	31	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (2s6p)	—	23	°C/W
$R_{\theta JB}$	Thermal Resistance Junction to Board (2s2p)	—	15	°C/W
$R_{\theta JB}$	Thermal Resistance Junction to Board (2s6p)	—	10	°C/W

Table 6. Thermal ratings*...continued*

Symbol	Description (Rating)	Min	Max	Unit
$R_{\theta JC\_BOT}$	Thermal Resistance Junction to Case Bottom (between the die and the solder pad on the bottom of the package)	—	1	°C/W
$R_{\theta JP\_TOP}$	Thermal Resistance Junction to Package Top (between package top and the junction temperature)	—	3	°C/W

13 Characteristics

Table 7. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} from V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Power Supply					
I_{SUP_NORMAL}	Current in Normal Mode, all regulators ON (I_{LOAD} = 0)	—	15	25	mA
$I_{SUP\_STANDBY}$	Current in Standby mode, all regulators OFF, except VBOS	—	5	10	mA
I_{SUP_LPOFF}	Current in LPOFF Mode, T_A < 85°C	—	10	32	µA
V_{SUP_UV7}	V_{SUP} 7V undervoltage threshold	7.2	7.5	7.8	V
T_{SUP_UV}	V_{SUP_UVH}, V_{SUP_UVL} and V_{SUP_UV7} filtering time	6.0	10	15	µs
V_{SUP_UVLP}	Low power V_{SUP} undervoltage threshold	3.4	3.65	3.9	V
V_{SUP_UVH}	V_{SUP} undervoltage threshold high (during power up and V_{SUP} rising) OTP VSUP_CFG = 0 OTP VSUP_CFG = 1	 4.5 6.0	 4.7 6.2	 4.9 6.4	V
V_{SUP_UVL}	VSUP undervoltage threshold low (during normal operation and V_{SUP} falling) OTP VSUP_CFG = 0 OTP VSUP_CFG = 1	 4.0 5.3	 4.2 5.5	 4.4 5.7	V
Power supply of 24 V battery network application part numbers (see Table 2)					
V_{SUP}	Device input supply voltage (on VSUP1/2 pins)	—	24	60	V
V_{SUP_OV}	V_{SUP} overvoltage threshold VSUP_OV_CFG = 0 VSUP_OV_CFG = 1	 30 48.5	 32 51	 34 54	V
Power supply of 12 V battery network application part numbers (see Table 2)					
V_{SUP}	Device input supply voltage (on VSUP1/2 pins)	—	12	36	V
V_{SUP_OV}	V_{SUP} overvoltage threshold OTP VSUP_OV_CFG = 0	 30	 32	 34	V
Interface supply pins					
V_{MON0_I2C}	VMON0_I2C supply voltage range	1.71	—	3.465	V

The V_{SUP_OV} comparator will trigger a flag in the I2C mapping for MCU diagnostic to indicate a load dump happened but will have no direct action to the safety pins (FS0B, RSTB, PGOOD).

14 Functional Description

The FS86 has two independent logic blocks, i.e. state machines. The main state machine manages the power management, the LPOFF/STANDBY states, and the wake-up sources. The Fail-safe state machine manages the monitoring of the power management, the monitoring of the MCU and the monitoring of an external IC.

14.1 Simplified functional state diagram

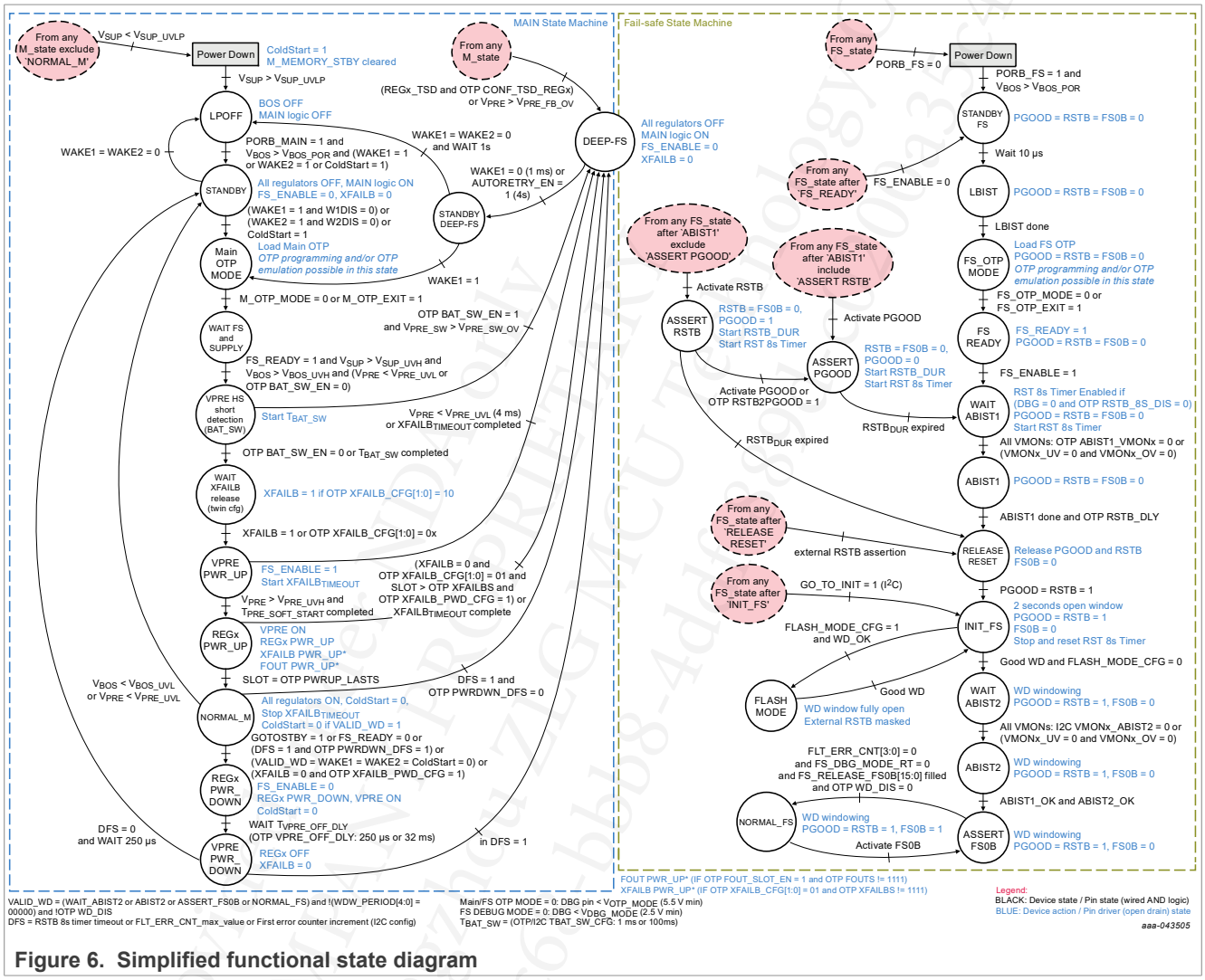


Figure 6. Simplified functional state diagram

14.2 Main state machine

The FS86 starts when VSUP1/2 pin voltage V_{SUP} > V_{SUP_UVH} and WAKE1 or WAKE2 pins voltages > $WAKE12_{VIH}$, except when first supplied where it starts regardless of WAKE1/2 pins state in a mode called Cold Start (ColdStart = 1). VBOS is the first supply to start, followed by VPRE, then power up sequencing from the OTP programming for the remaining regulators. If during the power-up sequence V_{SUP} < V_{SUP_UVL}, the device goes back to STANDBY state.. When the power up is finished, the main state machine is in NORMAL_M state, which is the application running mode with all the regulators ON and

V_{SUP_UVL} has no effect even if $V_{SUP} < V_{SUP\_UVL}$. ColdStart is reset in NORMAL_M state if OTP WD_DIS = 0. See Figure 4 for the minimum operating voltage.

The battery switch protection can be used to detect PRE HS MOS leakage before start-up sequence. If the battery switch protection is enabled (OTP BAT_SW_EN = 1), the device will monitor the VPRE switching node (PRE_SW pin voltage $V_{PRE\_SW} < V_{PRE\_SW\_OV}$) during T_{BAT_SW} (OTP/I2C TBAT_SW_CFG: 1 ms or 100 ms) before proceeding to VPRE power-up sequence and synchronization. The device goes DEEP-FS state if the $V_{PRE\_SW\_OV}$ threshold is reached within T_{BAT_SW}.

The power-up sequence can be synchronized with another PMIC using the XFAILB pin in order to stop before or after VPRE is ON and wait for the PMIC feedback on XFAILB pin before allowing FS86 to continue its power-up sequence. See Section 27 "XFAILB: Power synchronization" for more details on XFAILB pin.

If the VPRE power-up sequence is not completed ($V_{PRE} < V_{PRE\_UVL}$) within $T_{VPRE\_UV\_DFS}$ (4 ms), the device goes to DEEP-FS state. After start up is completed, in case of loss of VPRE ($V_{PRE} < V_{PRE\_UVL}$) or loss of VBOS ($V_{BOS} < V_{BOS\_UVL}$), the device goes directly to STANDBY state without power down sequence. In all these cases, VPRE restarts when $V_{SUP} > V_{SUP\_UVH}$ and WAKE1 or WAKE2 pins voltages > $WAKE12_{VIH}$.

The device can go to STANDBY state by a I^2C command from the MCU. If the WD is disabled by OTP WD_DIS bit for an application without MCU, the device goes to Standby mode when both WAKE1 and WAKE2 pins voltages < $WAKE12_{VIL}$. The device goes to STANDBY state following the power down sequence to stop all the regulators in the reverse order of the power-up sequence. VPRE shutdown can be delayed from 250 µs to 32 ms by VPRE_OFF_DLY bit in case VPRE is supplying an external PMIC to wait its power down sequence completion.

In case of $V_{PRE\_FB\_OV}$ detection, or TSD detection on a regulator depending on OTP CONF_TSD bits configuration, or deep fail-safe request from the fail-safe state machine when DFS = 1, the device stops and goes directly to DEEP-FS state without power down sequence.

Exit of DEEP-FS state is only possible by WAKE1 pin voltage $V_{WAKE1} < WAKE12_{VIL}$ for 1 ms or after 4 s if the autoretry feature is activated (OTP AUTORETRY_EN = 1). The number of autroretry can be limited to 15 or be infinite, depending on the OTP AUTORETRY_INFINITE bit. Device restarts the power-up sequence when $V_{SUP} > V_{SUP\_UVH}$ and $V_{WAKE1} > WAKE12_{VIH}$.

14.3 Fail-Safe state machine

The Fail-Safe state machine starts with LBIST execution when $V_{BOS} > V_{BOS\_POR}$. When the LBIST is done, the 8 s timer monitoring the RSTB pin is enabled, i.e. the main state machine goes to the DEEP-FS state if RSTB pin stays low longer than $RSTB_{T8S}$. The ABIST1 is automatically executed when all the regulators assigned to ABIST1 have passed their undervoltage threshold and remain under their overvoltage threshold. When the ABIST1 is done, RSTB and PGOOD pins are released and the initialization of the device is opened for 2 s. If the watchdog is not correctly refreshed within the 2 s window, RSTB is asserted and the fault error counter is incremented by 1. ABIST1 fail does not prevent RSTB and PGOOD release but maintains FS0B asserted.

The first good watchdog refresh closes the INIT_FS. Continuous watchdog refresh is then required. The device waits for the regulators assigned to ABIST2 in FS_I_VMON_ABIST2 register during INIT_FS to be started. When the ABIST2 is done and passes, the fault counter must be cleared with the appropriate number of good

watchdog refresh to release the FS0B pin per the procedure described in Section 31.9.4 "FS0B release".

When FS0B pin is released, the device is ready for application running mode with all the selected monitoring activated. From now on, the FS86 reacts by asserting the safety pins (PGOOD, RSTB and FS0B) according to its configuration when a fault is detected. The safety pins hierarchical priority is 1-PGOOD, 2-RSTB, 3-FS0B.

14.4 Power sequencing

VPRE is the first regulator to start automatically, then the other regulators start following the OTP power sequencing configuration. Fifteen slots are available, from SLOT_0 to SLOT_14, to program the start-up sequence of BOOST, BUCK, LDO1 and LDO2 regulators, as well as FOUT assertion to high and XFAILB release. The timing between each slot execution, T_{SLOT}, is configurable by OTP to accommodate the different system requirements. T_{SLOT} is set with OTP TSLOT[1:0] bits to 0.5 ms, 1 ms, 2 ms or 8 ms.

The power-up sequence starts at SLOT_0 towards SLOT_14 and stops at the last configured by OTP at PWRUP_LASTS[3:0]. The power-down sequence is executed in reverse order, starting in PWRDWN_FIRSTS[3:0] towards SLOT_0.

All regulators assigned to SLOT_15 are not started during the power-up sequence. These regulators can be started (or not) later when the main state machine is in NORMAL_M mode with an I2C command to write in M_REG_CTRL1 register if they were enabled by OTP.

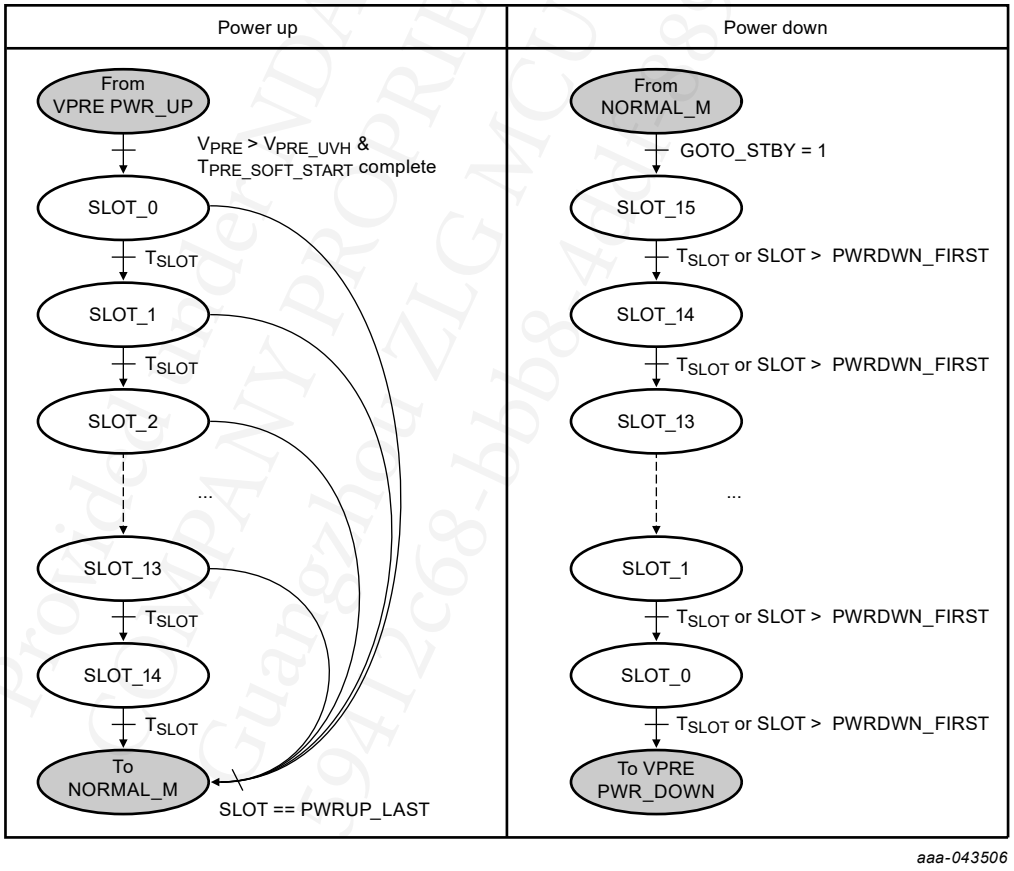


Figure 7. Power sequencing

Each regulator is assigned to a SLOT by OTP configuration using OTP BOOSTS[3:0] for BOOST, OTP BUCKS[3:0] for BUCK, OTP LDO1S[3:0] for LDO1 and OTP LDO2S[3:0] for LDO2, as well as FOUTS[3:0] for FOUT if configured in FOUT_SLOT_EN and XFAILBS[3:0] for XFAILB if configured in XFAILB_SLOT_CFG. After power-up sequence, FOUT and XFAILB can be placed in a different slot for the power down sequence using I2C registers FOUTS[3:0] and XFAILBS[3:0], respectively.

The different soft start durations of BOOST, BUCK and LDOs should be considered in the SLOT assignment to achieve the correct sequence with or without overlap. All slots after the last power up slot are bypassed to allow to shorten the power up duration if needed. All slots before the first power down slot are executed without T_{SLOT} wait time to force all the regulators OFF. As a result, the total power sequencing duration depends on the slot duration and the number of configured slots for power-up and power-down.

An additional delay can be added in the power down sequence before VPRE turn-OFF. VPRE turn-OFF delay $T_{VPRE\_OFF\_DLY}$ can be configured with OTP VPRE_OFF_DLY to 250 µs or 32 ms.

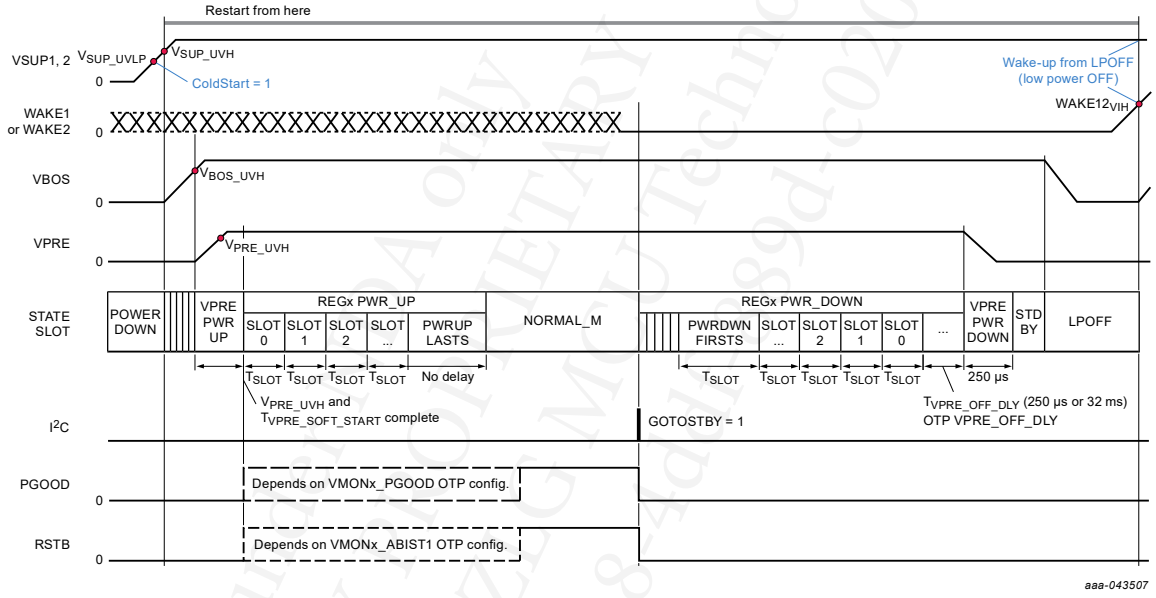


Figure 8. Power-up sequence example

Table 8. Slot assignment table

Slot code S[3:0]	Slot assignation
0000	SLOT_0
0001	SLOT_1
0010	SLOT_2
0011	SLOT_3
0100	SLOT_4
0101	SLOT_5
0110	SLOT_6
0111	SLOT_7
1000	SLOT_8

Table 8. Slot assignment table*...continued*

Slot code S[3:0]	Slot assignation
1001	SLOT_9
1010	SLOT_10
1011	SLOT_11
1100	SLOT_12
1101	SLOT_13
1110	SLOT_14
1111	SLOT_15 (regulators enabled by I2C)

14.4.1 Electrical characteristics

Table 9. Electrical characteristics

TA = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Power up sequencing					
T_{SLOT}	**Slot time**				ms
	TSLOT[1:0] = 00	0.47	0.5	0.53	
	TSLOT[1:0] = 01	0.94	1	1.06	
	TSLOT[1:0] = 10	1.88	2	2.12	
	TSLOT[1:0] = 11	7.52	8	8.48	

14.5 Debug and OTP modes

The FS86 enters fail-safe DEBUG mode when V_{DBG} (DBG pin voltage) > V_{DBG_MODE} after VBOS is started and before VPRE is enabled. It is recommended to connect DBG pin to VBOS through a diode ($V_{DBG} = V_{BOS} – Vd \approx 4.5$ V). The DEBUG mode disables the Watchdog windowing (fully opened window), the RSTB 8 s timer, the DEEP-FS state entry by the fail-safe state (DFS = 1), and locks FS0B low.

The FS86 enters main and fail-safe OTP mode when $V_{DBG} > V_{OTP\_MODE}$ before $V_{SUP} > V_{SUP\_UVH}$. It is recommended to apply V_{OTP_MODE} with an external power supply at the DBG pin before applying V_{SUP}. In this case, the diode protects VBOS. V_{OTP_MODE} must equal 7.95 V for the OTP programming process.

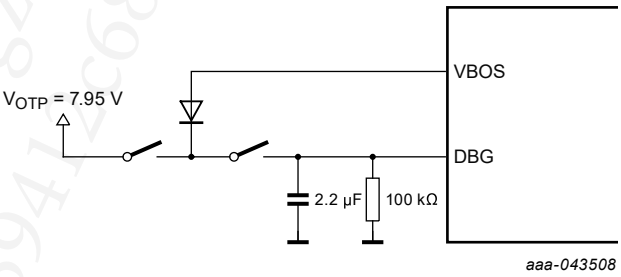


Figure 9. Debug pin (DBG) circuitry

14.5.1 Electrical characteristics

Table 10. Electrical Characteristics

TA = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Debug mode					
V_{DBG_MODE}	DEBUG Mode input threshold at DBG pin	2.5	3.0	3.5	V
	Voltage to apply at DBG pin to enter Debug mode	3.5	4.5	5.5	V
T_{DBG_MODE}	DEBUG Mode entry filtering time	4.0	5.5	7.0	µs
V_{OTP_MODE}	OTP Mode input threshold at DBG pin	5.5	6.0	6.5	V
	Voltage to apply at DBG pin to program the OTP	7.75	7.95	8.15	V
T_{OTP_MODE}	OTP Mode entry filtering time	4.0	5.5	7.0	µs
I_{DBG}	DBG pin input current consumption	—	—	60	µA

14.6 MCU flash mode

MCU flash mode is a specific state of the fail-safe state machine that can be entered by software from INIT_FS to flash the MCU in the field. Unlike Debug mode entry, no hardware configuration is required for MCU flash mode entry. In MCU flash mode, the Watchdog window is fully opened (no closed window) and external RSTB assertion is ignored.

FS86 enters FLASH mode when FLASH_MODE_CFG bit is set and INIT_FS is closed with a good Watchdog refresh. FS86 exits MCU flash mode and goes back to INIT_FS with a good Watchdog refresh (no RSTB assertion).

The watchdog window period can be disabled or extended in INIT_FS before going to the MCU flash mode. If the Watchdog window period is not extended to accommodate the programming time, customers will have to refresh it during the MCU programming and consequently exit MCU flash mode at the first good WD refresh. If a Watchdog refresh error occurs, the device exits the MCU flash mode and goes back to INIT_FS with a RSTB pulse.

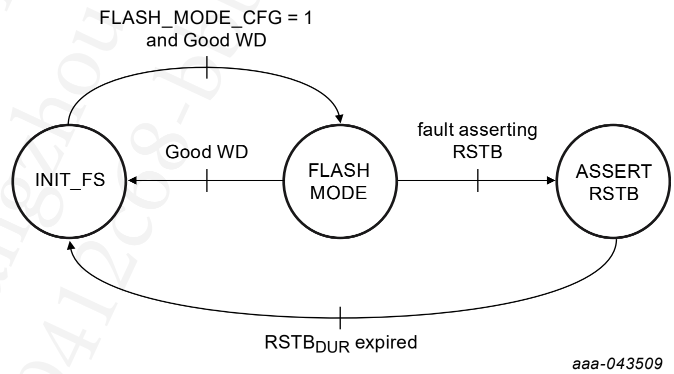


Figure 10. MCU flash mode states and transitions

14.7 Memory bits available in LPOFF state

FS86 has 19 bits available in LPOFF state. Their content is kept till a loss of battery supply. Customer can store data in 12 bits during LPOFF state.

The other seven bits have a dedicated function:

1. **BAT_FAIL** bit reports the battery disconnection.
2. **STBY** bit reports if the device resumes from LPOFF state after MCU GOTOSTBY request.
3. **XFAILB** bit reports if the device resumes from LPOFF/STANDBY state after XFAILB assertion.
4. **DFS** bit reports if the device resume from DEEP-FS state by a main state machine request.
5. **FS_DFS** bit reports if the device resumes from DEEP-FS state due to a fail-safe fault (DFS = 1).
6. **TSD_DFS** bit reports if the device resumes from DEEP-FS state due to a TSD fault on one of the regulators.
7. **TBAT_SW_CFG** bit configures the battery switch timer after next wake up from LPOFF/STANDBY state to change the OTP default configuration.

15 I^{2}C

15.1 I^{2}C interface overview

The FS86 uses an I^{2}C interface following the high-speed mode definition up to 1.0 Mbits per second. I^{2}C interface protocol requires a device address for addressing the target IC on a multi-device bus. The FS86 has two device addresses: one to access the main logic and one to access the fail-safe logic. These two I^{2}C addresses are set by OTP.

The I^{2}C interface is using a dedicated power input pin VMON0_I2C and it is compatible with 1.8 V and 3.3 V input supply. Timing, diagrams, and further details can be found in the NXP I^{2}C specification UM10204 rev6.

Table 11. I2C message structure

B39	B38	B37	B36	B35	B34	B33	B32
ID_6_0							R/W
Device Address							1 – Read 0 – Write
B31	**B30**	**B29**	**B28**	**B27**	**B26**	**B25**	**B24**
0	0	Adr_5-0					
Reserved		Register Address					
B23	**B22**	**B21**	**B20**	B19	B18	**B17**	**B16**
Data_15	Data_14	Data_13	Data_12	Data_11	Data_10	Data_9	Data_8
Data MSB							
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Data_7	Data_6	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
Data LSB							

Table 11. I2C message structure*...continued*

B39	B38	B37	B36	B35	B34	B33	B32
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0

An 8-bit CRC is required for each Write and Read I^2C command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two. The CRC polynomial used is compatible with SAE J1850 CRC8: x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

15.2 Device address

The FS86 has two device address: one to access the Main logic and one to access the Fail-safe logic.

Table 12. Device address structure

B39	B38	B37	B36	B35	B34	B33
0	1	OTP	OTP	OTP	OTP	M/FS

The I^2C addresses have the following arrangement:

- Bit 39: 0
- Bit 38: 1
- Bit 37 to 34: OTP value, see I2CDEVADDR[3:0] (main) and I2CDEVID[3:0] (Fail-Safe)
- Bit 33: 0 to access the main logic, 1 to access the fail-safe logic

15.3 I2C CRC calculation and results

CRC calculation using XOR:

- CRC_7 = XOR (B38, B35, B32, B31, B24, B23, B22, B20, B17, B13, B12, B11, 1, 1, 1)
- CRC_6 = XOR (B37, B34, B23, B22, B21, B19, B16, B12, B11, B10, 1, 1)
- CRC_5 = XOR (B39, B36, B33, B30, B29, B22, B21, B20, B18, B15, B11, B10, B9, 1, 1, 1)
- CRC_4 = XOR (B39, B38, B35, B32, B29, B28, B21, B20, B19, B17, B14, B10, B9, B8, 1, 1, 1, 1)
- CRC_3 = XOR (B37, B35, B34, B32, B28, B27, B24, B23, B22, B19, B18, B17, B16, B12, B11, B9, B8, 1, 1, 1, 1)
- CRC_2 = XOR (B39, B38, B36, B35, B34, B33, B32, B27, B26, B24, B21, B20, B18, B16, B15, B13, B12, B10, B8, 1, 1, 1, 1, 1, 1, 1)
- CRC_1 = XOR (B37, B34, B33, B26, B25, B24, B22, B19, B15, B14, B13, B9, 1, 1, 1)
- CRC_0 = XOR (B39, B36, B33, B32, B25, B24, B23, B21, B18, B14, B13, B12, B8, 1, 1, 1, 1)

CRC results examples:

- Main I^2C device address: 0x20
- Fail-safe I^2C device address: 0x21

Table 13. CRC results examples

Device address, R/W 8 bit (Hex)	Register address 8 bit (Hex)	Data MSB 8 bit (Hex)	Data LSB 8 bit (Hex)	CRC 8 bit (Hex)
0x40	0x02	0x00	0x00	0x31
0x42	0x01	0xD0	0x0D	0x8C

15.4 Electrical characteristics

Table 14. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
I2C					
VMON0_I2C	I2C interface power input VMON0_I2C_V = 0 VMON0_I2C_V = 1	 1.71 3.135	 1.8 3.3	 1.89 3.465	V
F_{SCL}	SCL clock frequency (Fast Mode Plus)	—	—	1.0	MHz
$I2C_{VIL}$	SCL, SDA Low level input voltage	0.3 x VMON0_I2C	—	—	V
$I2C_{VIH}$	SCL, SDA High level input voltage	—	—	0.7 x VMON0_I2C	V
$I2C_{th}$	SCL, SDA input hysteresis VMON0_I2C = 1.8 V VMON0_I2C = 3.3 V	 100 170	 —	 —	mV
SDA_{VOL}	Low level output voltage at SDA pin (I = 20 mA)	—	—	0.4	V
C_{I2C}	Input capacitance at SCL / SDA	—	—	10	pF
t_{SPSCL}	SCL pulse width filtering time, when 50 ns filter selected (Fast speed, Fast speed plus)	50	—	150	ns
t_{SPSDA}	SDA pulse width filtering time, when 50 ns filter selected (Fast speed, Fast speed plus)	50	—	150	ns
T_{VD_DAT}	Data valid time from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse) Standard Mode Fast Mode Fast Mode Plus	 —	 —	 3.34 0.90 0.45	µs

16 Register mapping

Table 15. Register mapping

Register	M/FS	Address						R/W I2C	Read / Write	Reference
		bit 5	bit 4	bit 3	bit 2	bit 1	bit 0			
M_FLAG	0	0	0	0	0	0	0	1/0	Read / Write	Section 17.3

Table 15. Register mapping*...continued*

Register	M/FS	Address						R/W I2C	Read / Write	Reference
		bit 5	bit 4	bit 3	bit 2	bit 1	bit 0			
M_MODE	0	0	0	0	0	0	1	1/0	Read / Write	Section 17.4
M_REG_CTRL1	0	0	0	0	0	1	0	1/0	Read / Write	Section 17.5
M_REG_CTRL2	0	0	0	0	0	1	1	1/0	Read / Write	Section 17.6
M_AMUX	0	0	0	0	1	0	0	1/0	Read / Write	Section 17.8
M_CLOCK	0	0	0	0	1	0	1	1/0	Read / Write	Section 17.7
M_INT_MASK1	0	0	0	0	1	1	0	1/0	Read / Write	Section 17.9
M_INT_MASK2	0	0	0	0	1	1	1	1/0	Read / Write	Section 17.10
M_FLAG1	0	0	0	1	0	0	0	1/0	Read / Write	Section 17.11
M_FLAG2	0	0	0	1	0	0	1	1/0	Read / Write	Section 17.12
M_FLAG3	0	0	0	1	0	1	0	1/0	Read / Write	Section 17.13
M_VMON1_REGX	0	0	0	1	0	1	1	1/0	Read / Write	Section 17.14
M_VMON2_REGX	0	0	0	1	1	0	0	1/0	Read / Write	Section 17.15
M_BAT_SW	0	0	0	1	1	0	1	1/0	Read / Write	Section 17.16
M_MEMORY	0	1	0	0	1	0	1	1/0	Read / Write	Section 17.17
M_MEMORY_STDY	0	1	0	0	1	1	0	1/0	Read / Write	Section 17.18
M_FLAG_STDY	0	1	0	0	1	1	1	1/0	Read / Write	Section 17.19
M_DEVICEID	0	1	0	1	0	0	0	1	Read only	Section 17.20
M_SYNC_SLOT	0	1	0	1	0	1	1	1/0	Read / Write	Section 17.21
FS_GRL_FLAGS	1	0	0	0	0	0	0	1	Read only	Section 17.21
FS_I_OVUV_SAFE_ REACTION1	1	0	0	0	0	0	1	1/0	Write during INIT then Read only	Section 18.4
FS_I_NOT_OVUV_ SAFE_REACTION1	1	0	0	0	0	1	0	1/0	Write during INIT then Read only	
FS_I_OVUV_SAFE_ REACTION2	1	0	0	0	0	1	1	1/0	Write during INIT then Read only	Section 18.5
FS_I_NOT_OVUV_ SAFE_REACTION2	1	0	0	0	1	0	0	1/0	Write during INIT then Read only	
FS_I_OVUV_SAFE_ REACTION3	1	0	0	0	1	0	1	1/0	Write during INIT then Read only	Section 18.6
FS_I_NOT_OVUV_ SAFE_REACTION3	1	0	0	0	1	1	0	1/0	Write during INIT then Read only	
FS_I_VMON_ABIST2	1	0	0	0	1	1	1	1/0	Write during INIT then Read only	Section 18.7
FS_I_NOT_VMON_ ABIST2	1	0	0	1	0	0	0	1/0	Write during INIT then Read only	
FS_I_WD_CFG	1	0	0	1	0	0	1	1/0	Write during INIT then Read only	Section 18.8
FS_I_NOT_WD_CFG	1	0	0	1	0	1	0	1/0	Write during INIT then Read only	
FS_I_SAFE_INPUTS	1	0	0	1	0	1	1	1/0	Write during INIT then Read only	Section 18.9
FS_I_NOT_SAFE_ INPUTS	1	0	0	1	1	0	0	1/0	Write during INIT then Read only	

Table 15. Register mapping*...continued*

Register	M/FS	Address						R/W I2C	Read / Write	Reference
		bit 5	bit 4	bit 3	bit 2	bit 1	bit 0			
FS_I_FSSM	1	0	0	1	1	0	1	1/0	Write during INIT then Read only	Section 18.10
FS_I_NOT_FSSM	1	0	0	1	1	1	0	1/0	Write during INIT then Read only	
FS_I_SVS1	1	0	0	1	1	1	1	1/0	Write during INIT then Read only	Section 18.11
FS_I_NOT_SVS1	1	0	1	0	0	0	0	1/0	Write during INIT then Read only	
FS_I_SVS2	1	0	1	0	0	0	1	1/0	Write during INIT then Read only	Section 18.12
FS_I_NOT_SVS2	1	0	1	0	0	1	0	1/0	Write during INIT then Read only	
FS_WD_WINDOW	1	0	1	0	0	1	1	1/0	Read / Write	Section 18.13
FS_NOT_WD_ WINDOW	1	0	1	0	1	0	0	1/0	Read / Write	
FS_WD_SEED	1	0	1	0	1	0	1	1/0	Read / Write	Section 18.14
FS_WD_ANSWER	1	0	1	0	1	1	0	0	Write only	Section 18.15
FS_OVUVREG_ STATUS1	1	0	1	0	1	1	1	1/0	Read / Write	Section 18.16
FS_OVUVREG_ STATUS2	1	0	1	1	0	0	0	1/0	Read / Write	Section 18.17
FS_RELEASE_FS0B	1	0	1	1	0	0	1	1/0	Read / Write	Section 18.18
FS_SAFE_IOS	1	0	1	1	0	1	0	1/0	Read / Write	Section 18.19
FS_DIAG_SAFETY	1	0	1	1	0	1	1	1/0	Read / Write	Section 18.20
FS_INTB_MASK	1	0	1	1	1	0	0	1/0	Read / Write	Section 18.21
FS_STATES	1	0	1	1	1	0	1	1/0	Read / Write	Section 18.22

17 Main register mapping

17.1 Main writing registers overview

Table 16. Main writing registers overview

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Main	M_FLAG	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	I2C_M_CRC	I2C_M_REQ
	M_MODE	0	VSUP_OV_CFG	FOUT_STATE	INTB_REQ	M_OTP_EXIT	0	EXT_FIN_SEL	0
		0	EXT_FIN_DIS	0	0	0	W2DIS	W1DIS	GOTOSTBY
	M_REG_CTRL1	VPRE_PD_DIS	VPREDIS	BOOSTDIS	0	0	BUCKDIS	LDO1DIS	LDO2DIS
		0	VPREEN	BOOSTEN	0	0	BUCKEN	LDO1EN	LDO2EN
	M_REG_CTRL2	VBSTSR[1:0]		BOOSTTSDCFG	0	0	BUCKTSDCFG	LDO1TSDCFG	LDO2TSDCFG
		VPRESRHS_RISE		0	VPRESRLS		0	VPRESRHS_FALL	
	M_AMUX	0	0	0	0	0	0	0	0
		0	0	RATIO	AMUX[4:0]				
	M_CLOCK	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
		FOUT_CLK_SEL	0	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
	M_INT_MASK1	0	VPREOC_M	0	0	0	BUCKOC_M	LDO1OC_M	LDO2OC_M
		0	0	BOOSTTSD_M	0	0	BUCKTSD_M	LDO1TSD_M	LDO2TSD_M
	M_INT_MASK2	0	0	0	0	VBOOSTOV_M	VBOSUVH_M	COM_M	VPREOV_M
		0	VSUPUV7_M	VSUPUOV_M	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
	M_FLAG1	VBOSUVH	0	VPREOC	0	0	BUCKOC	LDO1OC	LDO2OC
		0	VBOOSTOV	VBOOSTOT	0	0	BUCKOT	LDO1OT	LDO2OT
	M_FLAG2	VPREOV	VSUPUV7	0	0	0	0	0	0
		VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	0	0	WK2FLG	WK1FLG
	M_FLAG3	VSUP_OV	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0
	M_VMON1_REGX	0	VMON4_REG_ASSIGN[2:0]			VMON3_REG_ASSIGN[2:0]			VMON2_REG_ASSIGN[2]
		VMON2_REG_ASSIGN[1:0]		VMON1_REG_ASSIGN[2:0]			VMON0_REG_ASSIGN[2:0]		
	M_VMON2_REGX	0	VMON9_REG_ASSIGN[2:0]			VMON8_REG_ASSIGN[2:0]			VMON7_REG_ASSIGN[2]
		VMON7_REG_ASSIGN[1:0]		VMON6_REG_ASSIGN[2:0]			VMON5_REG_ASSIGN[2:0]		

Table 16. Main writing registers overview*...continued*

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	M_BAT_SW	0	0	0	0	0	0	0	BAT_SW_RELEASE
		0	BAT_SW_ASSERT	0	0	0	0	0	0
	M_MEMORY	MEMORY0[15:0]							
	M_MEMORY_STB	0	0	0	MEMORY_STB[12:0]				
	M_FLAG_STBY	0	0	0	0	0	0	0	0
		0	TBAT_SW_CFG	TSD_DFS	FS_DFS	DFS	XFAILB	STBY	BAT_FAIL
	M_SYNC_SLOT	0	0	0	0	0	0	0	FOUTS[3]
		FOUTS[2:0]			0	XFAILBS[3:0]			

17.2 Main reading registers overview

Table 17. Main reading registers overview

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Main	M_FLAG	COM_ERR	WU_G	VPRE_G	VBOOST_G	0	0	VBUCK_G	VLDO1_G
		VLDO2_G	VSUP_G	0	0	0	0	I2C_M_CRC	I2C_M_REQ
	M_MODE	0	VSUP_OV_CFG	FOUT_STATE	0	0	0	0	PLL_LOCK_RT
		EXT_FIN_SEL_RT	0	MAIN_NORMAL	0	0	W2DIS	W1DIS	0
	M_REG_CTRL1	VPRE_PD_DIS	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0
	M_REG_CTRL2	VBSTSR[1:0]		BOOSTTSDCFG	0	0	BUCKTSDCFG	LDO1TSDCFG	LDO2TSDCFG
		VPRESRHS_RISE		0	VPRESRLS		0	VPRESRHS_FALL	
	M_AMUX	0	0	0	0	0	0	0	0
		0	0	RATIO	AMUX[4:0]				
	M_CLOCK	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
		FOUT_CLK_SEL	0	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
	M_INT_MASK1	0	VPREOC_M	0	0	0	BUCKOC_M	LDO1OC_M	LDO2OC_M
		0	0	BOOSTTSD_M	0	0	BUCKTSD_M	LDO1TSD_M	LDO2TSD_M
	M_INT_MASK2	0	0	0	0	VBOOSTOV_M	VBOSUVH_M	COM_M	VPREOV_M
		0	VSUPUV7_M	VSUPUOV_M	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
	M_FLAG1	VBOSUVH	0	VPREOC	0	0	BUCKOC	LDO1OC	LDO2OC

Table 17. Main reading registers overview*...continued*

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
		FIN_CLKWD_OK	VBOOSTOV	VBOOSTOT	0	0	BUCKOT	LDO1OT	LDO2OT
	M_FLAG2	VPREOV	VSUPUV7	BOOST_ST	0	0	BUCK_ST	LDO1_ST	LDO2_ST
		VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	WK2RT	WK1RT	WK2FLG	WK1FLG
	M_FLAG3	VSUP_OV	0	XFAILB_RT	0	M_OTP_MODE_RT	0	0	0
		0	0	0	0	0	0	0	0
	M_VMON1_REGX	0	VMON4_REG_ASSIGN[2:0]			VMON3_REG_ASSIGN[2:0]			VMON2_REG_ ASSIGN[2]
		VMON2_REG_ASSIGN[1:0]		VMON1_REG_ASSIGN[2:0]			VMON0_REG_ASSIGN[2:0]		
	M_VMON2_REGX	0	VMON9_REG_ASSIGN[2:0]			VMON8_REG_ASSIGN[2:0]			VMON7_REG_ ASSIGN[2]
		VMON7_REG_ASSIGN[1:0]		VMON6_REG_ASSIGN[2:0]			VMON5_REG_ASSIGN[2:0]		
	M_BAT_SW	0	0	0	0	0	0	0	0
		0	0	0	0	0	BAT_SW_SNS	0	BAT_SW_DRV
	M_MEMORY	MEMORY0[15:0]							
	M_MEMORY1	0	0	0	MEMORY_STB[12:0]				
	M_FLAG_STBY	0	0	0	0	0	0	0	0
		0	TBAT_SW_CFG	TSD_DFS	FS_DFS	DFS	XFAILB	STBY	BAT_FAIL
	M_DEVICEID	M_FMREV[3:0]				M_MMREV[3:0]			
		M_DEVICEID[7:0]							
	M_SYNC_SLOT	0	0	0	0	0	0	0	FOUTS[3]
		FOUTS[2:0]			0	XFAILBS[3:0]			

17.3 M_FLAG register

When the device starts up, clear all the flags by writing 1s on all bits.

Table 18. M_FLAG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	COM_ERR	WU_G	VPRE_G	BOOST_G	0	0	BUCK_G	LDO1_G
Reset	0	1	1	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	I2C_M_CRC	I2C_M_REQ
Read	LDO2_G	VSUP_G	0	0	0	0	I2C_M_CRC	I2C_M_REQ
Reset	0	1	0	0	0	0	0	0

Table 19. M_FLAG register bit description

Bit	Symbol	Description	
15	COM_ERR	Report an error in the I2C communication **COM_ERR** = I2C_M_CRC or I2C_M_REQ or FS_COM_G	
		0	No failure
		1	Failure
		Reset condition: Real time information - cleared when all individual bits are cleared	
14	WU_G	Report a wake-up event by WAKE1 or WAKE2 **WU_G** = WK1FLG or WK2FLG	
		0	No wake event
		1	Wake event
		Reset condition: Real time information - cleared when all individual bits are cleared	
13	VPRE_G	Report an event on VPRE (status change or failure) **VPRE_G** = VPREOC or VPREUVH or VPREUVL or VPREOV	
		0	No event

Table 19. M_FLAG register bit description*...continued*

Bit	Symbol	Description	
		1	Event occurred
		Reset condition: Real time information - cleared when all individual bits are cleared	
12	BOOST_G	Report an event on BOOST (status change or failure) **BOOST_G** = BOOSTOT or BOOSTOV	
		0	No event
		1	Event occurred
		Reset condition: Real time information - cleared when all individual bits are cleared	
9	BUCK_G	Report an event on BUCK (status change or failure) **BUCK_G** = BUCKOC or BUCKOT	
		0	No event
		1	Event occurred
		Reset condition: Real time information - cleared when all individual bits are cleared	
8	LDO1_G	Report an event on LDO1 (status change or failure) **LDO1_G** = LDO1OC or LDO1OT	
		0	No event
		1	Event occurred
		Reset condition: Real time information	
7	LDO2_G	Report an event on LDO2 (status change or failure) **LDO2_G** = LDO2OC or LDO2OT	
		0	No event
		1	Event occurred
		Reset condition: Real time information	
6	VSUP_G	Report an event on VSUP (status change or failure) **VSUP_G** = VSUP_OV or VSUPUV7 or VSUPUVH or VSUPUVL	
		0	No event
		1	Event occurred
		Reset condition: Real time information	

Table 19. M_FLAG register bit description*...continued*

Bit	Symbol	Description	
1	I2C_M_CRC	Main domain I2C communication CRC issue	
		0	No error
		1	Error detected in the I2C CRC
		Reset condition: POR / clear on write (write '1')	
0	I2C_M_REQ	Invalid main domain I2C access (wrong Write or Read, Write to INIT registers in normal mode, wrong address)	
		0	No error
		1	I2C violation
		Reset condition: POR / clear on Write (write '1')	

17.4 M_MODE register

Table 20. M_MODE register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	VSUP_OV_CFG	FOUT_STATE	INTB_REQ	M_OTP_EXIT	0	EXT_FIN_SEL	0
Read	RESERVED	VSUP_OV_CFG	FOUT_STATE	0	0	0	0	PLL_LOCK_RT
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	EXT_FIN_DIS	0	0	0	W2DIS	W1DIS	GOTOSTBY
Read	EXT_FIN_SEL_RT	RESERVED	MAIN_NORMAL	RESERVED	RESERVED	W2DIS	W1DIS	RESERVED
Reset	0	0	1	0	0	0	0	0

Table 21. M_MODE register bit allocation

Bit	Symbol	Description	
14	VSUP_OV_CFG	VSUP OV threshold configuration	
		0	30V min - 32V typ - 34V max
		1	48.5V min - 51V typ - 54V max

Table 21. M_MODE register bit allocation...*continued*

Bit	Symbol	Description	
		Reset condition: POR	
13	FOUT_STATE	Drive FOUT state by I2C	
		0	Drive FOUT low state
		1	Drive FOUT high state
		Reset condition: POR	
12	INTB_REQ	Request assertion of INTB (pulse)	
		0	No effect
		1	INTB Assertion (pulse)
		Reset condition: POR	
11	M_OTP_EXIT	Leave Main OTP mode	
		0	No effect
		1	Leave Main OTP mode
		Reset condition: POR	
9	EXT_FIN_SEL	EXT FIN selection at PLL input request	
		0	No effect
		1	Request FIN selection
		Reset condition: POR	
8	PLL_LOCK_RT	Real time status of the PPL	
		0	PLL not locked
		1	PLL locked
		Reset condition: POR	
7	EXT_FIN_SEL_RT	Real time status of FIN clock selection	
		0	Internal clock oscillator is selected
		1	External FIN clock is selected
		Reset condition: POR	
6	EXT_FIN_DIS	Disable request of EXT FIN selection at PLL input	

Table 21. M_MODE register bit allocation*...continued*

Bit	Symbol	Description	
		0	No effect
		1	Disable FIN selection
		Reset condition: POR	
5	MAIN NORMAL	Main state machine status	
		0	Main state machine is not in Normal mode
		1	Main state machine is in Normal mode
		Reset condition: POR	
2	W2DIS	WAKE2 wake up disable	
		0	Wake up enable
		1	Wake up disable
		Reset condition: POR	
1	W1DIS	WAKE1 wake up disable	
		0	Wake up enable
		1	Wake up disable
		Reset condition: POR	
0	GOTOSTBY	Standby mode request	
		0	Device remains in current state
		1	Device enters in Standby mode
		Reset condition: POR	

17.5 M_REG_CTRL1 register

Table 22. M_REG_CTRL1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VPRE_PD_DIS	VPREDIS	BOOSTDIS	0	0	BUCKDIS	LDO1DIS	LDO2DIS
Read	VPRE_PD_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 22. M_REG_CTRL1 register bit allocation...*continued*

Bit	7	6	5	4	3	2	1	0
Write	0	VPREEN	BOOSTEN	0	0	BUCKEN	LDO1EN	LDO2EN
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 23. M_REG_CTRL1 register bit description

Bit	Symbol	Description	
15	VPRE_PD_DIS	Force disable of VPRE pull down	
		0	No effect (VPRE pull down is automatically controlled by the logic)
		1	VPRE pull down disable request
		Reset condition: POR	
14	VPREDIS	Disable request of VPRE	
		0	No effect (regulator remains in existing state)
		1	VPRE disable request
		Reset condition: POR	
13	BOOSTDIS	Disable request of BOOST	
		0	No effect (regulator remains in existing state)
		1	BOOST disable request
		Reset condition: POR	
10	BUCKDIS	Disable request of BUCK	
		0	No effect (regulator remains in existing state)
		1	BUCK disable request
		Reset condition: POR	
9	LDO1DIS	Disable request of LDO1	
		0	No effect (regulator remains in existing state)
		1	LDO1 disable request

Table 23. M_REG_CTRL1 register bit description*...continued*

Bit	Symbol	Description	
		Reset condition: POR	
8	LDO2DIS	Disable request of LDO2	
		0	no effect (regulator remains in existing state)
		1	LDO2 disable request
		Reset condition: POR	
6	VPREEN	Enable request of VPRE	
		0	No effect (regulator remains in existing state)
		1	VPRE enable request (after a VPDIS request)
		Reset condition: POR	
5	BOOSTEN	Enable request of BOOST	
		0	No effect (regulator remains in existing state)
		1	BOOST enable request
		Reset condition: POR	
2	BUCKEN	Enable request of BUCK	
		0	No effect (regulator remains in existing state)
		1	BUCK enable request
		Reset condition: POR	
1	LDO1EN	Enable request of LDO1	
		0	No effect (regulator remains in existing state)
		1	LDO1 enable request
		Reset condition: POR	
0	LDO2EN	Enable request of LDO2	
		0	no effect (regulator remains in existing state)
		1	LDO2 enable request
		Reset condition: POR	

17.6 M_REG_CTRL2 register

Table 24. M_REG_CTRL2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VBSTSR[1:0]		BOOSTTSDCFG	0	0	BUCKTSDCFG	LDO1TSDCFG	LDO2TSDCFG
Read	VBSTSR[1:0]		BOOSTTSDCFG	RESERVED	RESERVED	BUCKTSDCFG	LDO1TSDCFG	LDO2TSDCFG
Reset	OTP	OTP	OTP	0	0	OTP	OTP	OTP
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VPRESRHS_RISE[1:0]		0	VPRESRLS[1:0]		0	VPRESRHS_FALL[1:0]	
Read	VPRESRHS_RISE[1:0]		RESERVED	VPRESRLS[1:0]		RESERVED	VPRESRHS_FALL[1:0]	
Reset	OTP	OTP	0	OTP	OTP	0	OTP	OTP

Table 25. M_REG_CTRL2 register bit description

Bit	Symbol	Description	
15 to 14	VBSTSR[1:0]	VBOOST low-side slew rate control	
		00	50 V/µs – slow
		01	100 V/µs – medium
		10	300 V/µs – fast
		11	500 V/µs – ultra fast
		Reset condition: POR	
13	BOOSTTSDCFG	BOOST behavior in case of TSD	
		0	Regulator shutdown
		1	Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR	
10	BUCKTSDCFG	BUCK behavior in case of TSD	
		0	Regulator shutdown
		1	Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR	

Table 25. M_REG_CTRL2 register bit description*...continued*

Bit	Symbol	Description	
9	LDO1TSDCFG	LDO1 behavior in case of TSD	
		0	Regulator shutdown
		1	Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR	
8	LDO2TSDCFG	LDO2 behavior in case of TSD	
		0	Regulator shutdown
		1	Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR	
7 to 6	VPRESRHS_RISE[1:0]	VPRE high-side turn-ON slew rate control	
		00	130 mA typical drive capability - slow
		01	260 mA typical drive capability - medium
		10	520 mA typical drive capability - fast
		11	900 mA typical drive capability - ultra fast
		Reset condition: POR	
4 to 3	VPRESRLS[1:0]	VPRE low-side turn-ON and turn-OFF slew rate control	
		00	130 mA typical drive capability - slow
		01	260 mA typical drive capability - medium
		10	520 mA typical drive capability - fast
		11	900 mA typical drive capability - ultra fast
		Reset condition: POR	
1 to 0	VPRESRHS_FALL[1:0]	VPRE high-side turn-OFF slew rate control	
		00	130 mA typical drive capability - slow
		01	260 mA typical drive capability - medium
		10	520 mA typical drive capability - fast
		11	900 mA typical drive capability - ultra fast
		Reset condition: POR	

17.7 M_AMUX register

Table 26. M_AMUX register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	RATIO	AMUX[4:0]				
Read	RESERVED	RESERVED	RATIO	AMUX[4:0]				
Reset	0	0	0	0	0	0	0	0

Table 27. M_AMUX register bit description

Bit	Symbol	Description	
5	RATIO	Selection of divider ratio for Vsup, Wake1 and Wake 2 inputs	
		0	Ratio = 12
		1	Ratio = 24
		Reset condition: POR	
4 to 0	AMUX[4:0]	See Table 135	

17.8 M_CLOCK register

Table 28. M_CLOCK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
Read	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
Reset	OTP	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FOUT_CLK_SEL	0	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			

Table 28. M_CLOCK register bit allocation*...continued*

Read	FOUT_CLK_SEL	RESERVED	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
Reset	0	0	0	OTP	0	0	0	0

Table 29. M_CLOCK register bit description

Bit	Symbol	Description	
15	MOD_CONF	Modulation configuration of main oscillator	
		0	Triangular modulation (range -10%/0%, 19 kHz)
		1	Pseudo random modulation (range -10%/0%, 19 kHz/random)
		Reset condition: POR	
14 to 11	FOUT_MUX_SEL[3:0]	See Table 145	
10 to 8	FOUT_PH[2:0]	FOUT phase shifting configuration (see Section 30.2 "Phase shifting")	
		See Table 142	
		Reset condition: POR	
7	FOUT_CLK_SEL	FOUT_clk frequency selection (CLK1 or CLK2)	
		0	FOUT_clk = CLK1
		1	FOUT_clk = CLK2
		Reset condition: POR	
5	FIN_DIV	FIN input signal divider selection	
		0	Divider by 1
		1	Divider by 6
		Reset condition: POR	
4	MOD_EN	Modulation activation of main oscillator	
		0	Modulation disabled
		1	Modulation enabled
		Reset condition: POR	
3 to 0	CLK_TUNE[3:0]	Manual clock tuning (See Section 30.3 "Manual frequency tuning")	

Table 29. M_CLOCK register bit description...*continued*

Bit	Symbol	Description
		See Table 143

17.9 M_INT_MASK1 register

Table 30. M_INT_MASK1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	VPREOC_M	0	0	0	BUCKOC_M	LDO1OC_M	LDO2OC_M
Read	RESERVED	VPREOC_M	RESERVED	RESERVED	RESERVED	BUCKOC_M	LDO1OC_M	LDO2OC_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	BOOSTTSD_M	0	0	BUCKTSD_M	LDO1TSD_M	LDO2TSD_M
Read	RESERVED	RESERVED	BOOSTTSD_M	RESERVED	RESERVED	BUCKTSD_M	LDO1TSD_M	LDO2TSD_M
Reset	0	0	0	0	0	0	0	0

Table 31. M_INT_MASK1 register bit description

Bit	Symbol	Description	
14	VPREOC_M	Inhibit INTERRUPT for VPRE overcurrent	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
10	BUCKOC_M	Inhibit INTERRUPT for BUCK overcurrent	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
9	LDO1OC_M	Inhibit INTERRUPT for LDO1 overcurrent	
		0	INT not masked

Table 31. M_INT_MASK1 register bit description*...continued*

Bit	Symbol	Description	
		1	INT masked
		Reset condition: POR	
8	LDO2OC_M	Inhibit INTERRUPT for LDO2 overcurrent	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
5	BOOSTTSD_M	Inhibit INTERRUPT for BOOST overtemperature shutdown event	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
2	BUCKTSD_M	Inhibit INTERRUPT for BUCK overtemperature shutdown event	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
1	LDO1TSD_M	Inhibit INTERRUPT for LDO1 overtemperature shutdown event	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
0	LDO2TSD_M	Inhibit INTERRUPT for LDO2 overtemperature shutdown event	
		0	INT not masked
		1	INT masked
		Reset condition: POR	

17.10 M_INT_MASK2 register

Table 32. M_INT_MASK2 register bit allocation

Bit	15	14	13	12	11	10	9	8

Table 32. M_INT_MASK2 register bit allocation*...continued*

Write	0	0	0	0	VBOOSTOV_M	VBOSUVH_M	COM_M	VPREOV_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	VBOOSTOV_M	VBOSUVH_M	COM_M	VPREOV_M
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	VSUPUV7_M	VSUPOV_M	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
Read	RESERVED	VSUPUV7_M	VSUPOV_M	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
Reset	0	0	0	0	0	0	0	0

Table 33. M_INT_MASK2 register bit description

Bit	Symbol	Description	
11	VBOOSTOV_M	Inhibit INTERRUPT for VBOOST_OV any transition	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
10	VBOSUVH_M	Inhibit INTERRUPT for VBOS_UVH any transition	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
9	COM_M	Inhibit INTERRUPT for COM any transition	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
8	VPREOV_M	Inhibit INTERRUPT for VPRE_OV	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
7	VBOOSTUVH_M	Inhibit INTERRUPT for VBOOST_UVH	

Table 33. M_INT_MASK2 register bit description*...continued*

Bit	Symbol	Description	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
6	VSUPUV7_M	Inhibit INTERRUPT for VSUP_UV7	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
5	VSUPOV_M	Inhibit INTERRUPT for VSUP_OV	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
4	VSUPUVH_M	Inhibit INTERRUPT for VSUP_UVH	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
3	VSUPUVL_M	Inhibit INTERRUPT for VSUP_UVL	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
2	VPREUVH_M	Inhibit INTERRUPT for VPRE_UVH	
		0	INT not masked
		1	INT masked
		Reset condition: POR	
1	WAKE1_M	Inhibit INTERRUPT for WAKE1 any transition	
		0	INT not masked
		1	INT masked

Table 33. M_INT_MASK2 register bit description...*continued*

Bit	Symbol	Description	
		Reset condition: POR	
0	WAKE2_M	Inhibit INTERRUPT for WAKE2 any transition	
		0	INT not masked
		1	INT masked
		Reset condition: POR	

17.11 M_FLAG1 register

When the device starts up, clear all the flags by writing 1s on all bits.

Table 34. M_FLAG1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VBOSUVH	0	VPREOC	0	0	BUCKOC	LDO1OC	LDO2OC
Read	VBOSUVH	RESERVED	VPREOC	RESERVED	RESERVED	BUCKOC	LDO1OC	LDO2OC
Reset	1	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	VBOOSTOV	VBOOSTOT	0	0	BUCKOT	LDO1OT	LDO2OT
Read	FIN_CLKWD_OK	VBOOSTOV	VBOOSTOT	RESERVED	RESERVED	BUCKOT	LDO1OT	LDO2OT
Reset	0	0	0	0	0	0	0	0

Table 35. Table 30. M_FLAG1 register bit description

Bit	Symbol	Description	
15	VBOSUVH	VBOS undervoltage high event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
13	VPREOC	VPRE overcurrent event	

Table 35. Table 30. M_FLAG1 register bit description*...continued*

Bit	Symbol	Description	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
10	BUCKOC	BUCK overcurrent	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
9	LDO1OC	LDO2 overcurrent	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
8	LDO2OC	LDO1 overcurrent	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
7	FIN_CLKWD_OK	CLK_FIN_DIV monitoring	
		0	Not OK: CLK_FIN_DIV < FIN_{ERR_SLOW} or CLK_FIN_DIV > FIN_{ERR_FAST}
		1	OK: FIN_{ERR_SLOW} < CLK_FIN_DIV < FIN_{ERR_FAST}
		Reset condition: Real time information	
6	VBOOSTOV	VBOOST overvoltage protection event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
5	VBOOSTOT	VBOOST overtemperature shutdown event	
		0	No event
		1	Event occurred

Table 35. Table 30. M_FLAG1 register bit description*...continued*

Bit	Symbol	Description	
		Reset condition: POR / Clear on Write (write ‘1’)	
2	BUCKOT	BUCK overtemperature shutdown event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
1	LDO1OT	LDO1 overtemperature shutdown event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
0	LDO2OT	LDO2 overtemperature shutdown event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	

17.12 M_FLAG2 register

When the device starts up, clear all the flags by writing 1s on all bits.

Table 36. M_FLAG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VPREOV	VSUPUV7	0	0	0	0	0	0
Read	VPREOV	VSUPUV7	BOOST_ST	RESERVED	RESERVED	BUCK_ST	LDO1_ST	LDO2_ST
Reset	0	1	X	0	0	X	X	X
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	0	0	WK2FLG	WK1FLG
Read	VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	WK2RT	WK1RT	WK2FLG	WK1FLG
Reset	1	1	1	1	X	X	X	X

Table 37. M_FLAG2 register bit description

Bit	Symbol	Description	
15	VPREOV	VPRE_OV event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
14	VSUPUV7	VSUP_UV7 event (falling edge)	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
13	BOOST_ST	BOOST state	
		0	Regulator OFF
		1	Regulator ON
		Reset condition: Real time information	
10	BUCK_ST	BUCK state	
		0	Regulator OFF
		1	Regulator ON
		Reset condition: Real time information	
9	LDO1_ST	LDO1 state	
		0	regulator OFF
		1	regulator ON
		Reset condition: Real time information	
8	LDO2_ST	LDO2 state	
		0	regulator OFF
		1	regulator ON
		Reset condition: Real time information	
7	VPREUVL	VPRE_UVL event (falling edge)	
		0	No event

Table 37. M_FLAG2 register bit description*...continued*

Bit	Symbol	Description	
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
6	VPREUVH	VPRE_UVH event (rising edge)	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
5	VSUPUVL	VSUP_UVL event (falling edge)	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
4	VSUPUVH	VSUP_UVH event (rising edge)	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	
3	WK2RT	Report event: WAKE2 real time state	
		0	WAKE2 is low level
		1	WAKE2 is high
		Reset condition: Real time information	
2	WK1RT	Report event: WAKE1 real time state	
		0	WAKE1 is low level
		1	WAKE1 is high
		Reset condition: Real time information	
1	WK2FLG	WAKE2 wake up source flag (rising edge)	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)	

Table 37. M_FLAG2 register bit description*...continued*

Bit	Symbol	Description	
0	WK1FLG	WAKE1 wake up source flag (rising edge)	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write '1')	

17.13 M_FLAG3 register

When the device starts up, clear all the flags by writing 1s on all bits.

Table 38. M_FLAG3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VSUPOV	0	0	0	0	0	0	0
Read	VSUPOV	RESERVED	XFAILB_RT	RESERVED	M_OTP_ MODE_RT	RESERVED	RESERVED	RESERVED
Reset	0	0	X	0	X	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Note: *Reset value for FS86xx, wake up by Wake1, all regulators started by default during power-up sequence.*

Table 39. M_FLAG3 register bit description

Bit	Symbol	Description	
15	VSUPOV	VSUP_OV event	
		0	No event
		1	Event occurred
		Reset condition: POR / Clear on Write (write '1')	
13	XFAILB_RT	Report event: XFAILB real time state	

Table 39. M_FLAG3 register bit description*...continued*

Bit	Symbol	Description	
		0	XFAILB is low level
		1	XFAILB is high level
		Reset condition: Real time information	
11	M_OTP_MODE_RT	Real time status of Main OTP mode	
		Not in Main OTP mode	
		In Main OTP mode	
		POR	

17.14 M_VMON1_REGX register

Table 40. M_VMON1_REGX register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	VMON4_REG_ASSIGN[2:0]			VMON3_REG_ASSIGN[2:0]			VMON2_REG_ASSIGN[2]
Read	RESERVED	VMON4_REG_ASSIGN[2:0]			VMON3_REG_ASSIGN[2:0]			VMON2_REG_ASSIGN[2]
Reset	0	OTP	OTP	OTP	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON2_REG_ASSIGN[1:0]		VMON1_REG_ASSIGN[2:0]			VMON0_REG_ASSIGN[2:0]		
Read	VMON2_REG_ASSIGN[1:0]		VMON1_REG_ASSIGN[2:0]			VMON0_REG_ASSIGN[2:0]		
Reset	0	0	OTP	OTP	OTP	OTP	OTP	OTP

Table 41. M_VMON1_REGX register bit description

Bit	Symbol	Description
14 to 12	VMON4_REG_ASSIGN[2:0]	Regulator assignment to VMON4
		See Table 169
		Reset condition: POR
11 to 9	VMON3_REG_ASSIGN[2:0]	Regulator assignment to VMON3
		See Table 169
		Reset condition: POR
8 to 6	VMON2_REG_ASSIGN[2:0]	Regulator assignment to VMON2
		See Table 169
		Reset condition: POR
5 to 3	VMON1_REG_ASSIGN[2:0]	Regulator assignment to VMON1
		See Table 169
		Reset condition: POR
2 to 0	VMON0_REG_ASSIGN[2:0]	Regulator assignment to VMON0
		See Table 169

Table 41. M_VMON1_REGX register bit description*...continued*

Bit	Symbol	Description
		Reset condition: POR

17.15 M_VMON2_REGX register

Table 42. M_VMON_REG2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	VMON9_REG_ASSIGN[2:0]			VMON8_REG_ASSIGN[2:0]			VMON7_REG_ASSIGN[2]
Read	RESERVED	VMON9_REG_ASSIGN[2:0]			VMON8_REG_ASSIGN[2:0]			VMON7_REG_ASSIGN[2]
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON7_REG_ASSIGN[1:0]		VMON6_REG_ASSIGN[2:0]			VMON5_REG_ASSIGN[2:0]		
Read	VMON7_REG_ASSIGN[1:0]		VMON6_REG_ASSIGN[2:0]			VMON5_REG_ASSIGN[2:0]		
Reset	0	0	0	0	0	0	0	0

Table 43. M_VMON2_REGX register bit description

Bit	Symbol	Description
14 to 12	VMON9_REG_ASSIGN[2:0]	Regulator assignment to VMON9
		See Table 169
		Reset condition: POR
11 to 9	VMON8_REG_ASSIGN[2:0]	Regulator assignment to VMON8
		See Table 169
		Reset condition: POR
8 to 6	VMON7_REG_ASSIGN[2:0]	Regulator assignment to VMON7
		See Table 169
		Reset condition: POR
5 to 3	VMON6_REG_ASSIGN[2:0]	Regulator assignment to VMON6
		See Table 169
		Reset condition: POR
2 to 0	VMON5_REG_ASSIGN[2:0]	Regulator assignment to VMON5
		See Table 169

Table 43. M_VMON2_REGX register bit description*...continued*

Bit	Symbol	Description
		Reset condition: POR

17.16 M_BAT_SW register

When the device starts up, clear all the flags by writing 1s on all bits.

Table 44. M_BAT_SW register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	BAT_SW_ RELEASE
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	BAT_SW_ASSERT	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BAT_SW_SNS	RESERVED	BAT_SW_DRV
Reset	0	0	0	0	0	X	0	X

Table 45. M_FLAG2 register bit description

Bit	Symbol	Description	
8	BAT_SW_RELEASE	BAT_SW pin release request	
		0	No effect
		1	BAT_SW pin release request
		Reset condition: POR	
6	BAT_SW_ASSERT	BAT_SW pin assertion request	
		0	No effect
		1	BAT_SW pin assertion request
		Reset condition: POR	

Table 45. M_FLAG2 register bit description*...continued*

Bit	Symbol	Description	
2	BAT_SW_SNS	Report event: BAT_SW real time state	
		0	BAT_SW is low level
		1	BAT_SW is high
		Reset condition: Real time information	
0	BAT_SW_DRV	Report event: BAT_SW driver real time state	
		0	BAT_SW driver is low level
		1	BAT_SW driver is high
		Reset condition: Real time information	

17.17 M_MEMORY register

Table 46. M_MEMORY register bit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	MEMORY[15:0]															
Read	MEMORY[15:0]															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 47. M_MEMORY register bit description

Bit	Symbol	Description	
15 to 0	MEMORY[15:0]	Free memory field for data storage	
		0x0000 to 0xFFFF	16 bits free memory
		Reset condition: POR	

17.18 M_MEMORY_STBY register

Table 48. M_MEMORY_STBY register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	0	0	0	M_MEMORY_STBY[12:0]												
Read	RESERVED			M_MEMORY_STBY[12:0]												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 49. M_MEMORY_STBY register bit description

Bit	Symbol	Description	
12 to 0	M_MEMORY_STBY[12:0]	Free memory field for data storage	
		0x0000 to 0x1FFF	13 bits free memory
		Reset condition: VSUP < V_{SUP_UVLP}	

17.19 M_FLAG_STBY register

When the device starts up, clear all the flags by writing 1s on all bits.

Table 50. M_FLAG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	TBAT_SW_CFG	TSD_DFS	FS_DFS	DFS	XFAILB	STBY	BAT_FAIL
Read	RESERVED	TBAT_SW_CFG	TSD_DFS	FS_DFS	DFS	XFAILB	STBY	BAT_FAIL
Reset	0	0	0	0	0	0	0	1

Table 51. M_FLAG_STBY register bit description

Bit	Symbol	Description	
6	TBAT_SW_CFG	Battery switch timer selection	
		0	OTP TBAT_SW_CFG
		1	NOT OTP TBAT_SW_CFG
		Reset condition: VSUP < V_{SUP_UVLP}	
5	TSD_DFS	Report if the device resume from DEEP-FS state due to TSD event (Set to high only if regulator TSD & regulator CONF_TSD = 1)	
		0	No event
		1	Resume from DEEP-FS state due to TSD
		Reset condition: VSUP < V_{SUP_UVLP}	
4	FS_DFS	Report if the device resume from deep fail-safe mode due to FailSafe fault (DFS = 1)	
		0	No event
		1	Resume fromDEEP-FS state due to FailSafe
		Reset condition: VSUP < V_{SUP_UVLP}	

Table 51. M_FLAG_STBY register bit description*...continued*

Bit	Symbol	Description	
3	DFS	Report if the device resume from deep fail-safe mode (went thru DEEP-FS state)	
		0	No event
		1	Resume from deep fail-safe
		Reset condition: VSUP < V_{SUP_UVLP}	
2	XFAILB	Report if the device resume from Standby due to XFAILB (At NORMAL_M state, then XFAILB = 0 & XFAILB_PWD_CFG = 1)	
		0	No event
		1	Resume from STBY due to XFAILB
		Reset condition: VSUP < V_{SUP_UVLP}	
1	STBY	Report if the device resume from Standby due to MCU (At NORMAL_M state & GOTOSTBY = 1)	
		0	No event
		1	Resume from STBY
		Reset condition: VSUP < V_{SUP_UVLP}	
0	BAT_FAIL	Report the battery (VBAT) disconnection (POR of the low power logic when VSUP < V_{SUP_UVLP})	
		0	No event
		1	POR occurred
		Reset condition: VSUP < V_{SUP_UVLP}	

17.20 M_DEVICEID register

Table 52. M_DEVICEID register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	M_FMREV[3:0]				M_MMREV[3:0]			
Reset	0	0	0	0	0	0	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	M_DEVICEID[7:0]							

Table 52. M_DEVICEID register bit allocation...*continued*

Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

Table 53. M_DEVICEID register bit description

Bit	Symbol	Description	
15 to 12	M_FMREV[3:0]	Full mask revision configured by metal connection	
		0000	A silicon
11 to 8	M_MMREV[3:0]	Metal mask revision configured by metal connection	
		0000	0
		0001	1
7 to 0	M_DEVICEID[7:0]	Device ID from OTP DEVICEID[7:0] bits	
		Reset condition: POR	

17.21 M_SYNC_SLOT register

Table 54. M_SYNC_SLOT register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	FOUTS[3]
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FOUTS[3]
Reset	0	0	0	0	0	0	0	OTP
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FOUTS[2:0]			0	XFAILBS[3:0]			
Read	FOUTS[2:0]			RESERVED	XFAILBS[3:0]			
Reset	OTP	OTP	OTP	0	OTP	OTP	OTP	OTP

Table 55. M_SYNC_SLOT register bit description

Bit	Symbol	Description
8 to 5	FOUTS[3:0]	FOUT sequencing assertion (power down) slot

Table 55. M_SYNC_SLOT register bit description...*continued*

Bit	Symbol	Description
		See Table 8 default value is set by OTP.
3 to 0	XFAILBS[3:0]	XFAILB sequencing assertion (power down) slot
		See Table 8 default value is set by OTP.

18 Fail-Safe register mapping

18.1 Fail-Safe writing registers overview

Table 56. Fail-Safe writing registers overview

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Fail-safe	FS_I_OVUV_SAFE_REACTION1	VMON9_OV_IMPACT[1:0]		VMON9_UV_IMPACT[1:0]		VMON8_OV_IMPACT[1:0]		VMON8_UV_IMPACT[1:0]	
		VMON7_OV_IMPACT[1:0]		VMON7_UV_IMPACT[1:0]		VMON6_OV_IMPACT[1:0]		VMON6_UV_IMPACT[1:0]	
	FS_I_NOT_OVUV_SAFE_REACTION1	NOT_VMON9_OV_IMPACT[1:0]		NOT_VMON9_UV_IMPACT[1:0]		NOT_VMON8_OV_IMPACT[1:0]		NOT_VMON8_UV_IMPACT[1:0]	
		NOT_VMON7_OV_IMPACT[1:0]		NOT_VMON7_UV_IMPACT[1:0]		NOT_VMON6_OV_IMPACT[1:0]		NOT_VMON6_UV_IMPACT[1:0]	
	FS_I_OVUV_SAFE_REACTION2	VMON5_OV_IMPACT[1:0]		VMON5_UV_IMPACT[1:0]		VMON4_OV_IMPACT[1:0]		VMON4_UV_IMPACT[1:0]	
		VMON3_OV_IMPACT[1:0]		VMON3_UV_IMPACT[1:0]		VMON2_OV_IMPACT[1:0]		VMON2_UV_IMPACT[1:0]	
	FS_I_NOT_OVUV_SAFE_REACTION2	NOT_VMON5_OV_IMPACT[1:0]		NOT_VMON5_UV_IMPACT[1:0]		NOT_VMON4_OV_IMPACT[1:0]		NOT_VMON4_UV_IMPACT[1:0]	
		NOT_VMON3_OV_IMPACT[1:0]		NOT_VMON3_UV_IMPACT[1:0]		NOT_VMON2_OV_IMPACT[1:0]		NOT_VMON2_UV_IMPACT[1:0]	
	FS_I_OVUV_SAFE_REACTION3	VMON1_OV_IMPACT[1:0]		VMON1_UV_IMPACT[1:0]		0	0	0	0
		0	0	0	0	VMON0_OV_IMPACT[1:0]		VMON0_UV_IMPACT[1:0]	
	FS_I_NOT_OVUV_SAFE_REACTION3	NOT_VMON1_OV_IMPACT[1:0]		NOT_VMON1_UV_IMPACT[1:0]		0	0	0	0
		0	0	0	0	NOT_VMON0_OV_IMPACT[1:0]		NOT_VMON0_UV_IMPACT[1:0]	
	FS_I_VMON_ABIST2	0	0	0	0	0	0	VMON9_ABIST2	VMON8_ABIST2
		VMON7_ABIST2	VMON6_ABIST2	VMON5_ABIST2	VMON4_ABIST2	VMON3_ABIST2	VMON2_ABIST2	VMON1_ABIST2	VMON0_ABIST2
	FS_I_NOT_VMON_ABIST2	0	0	0	0	0	0	NOT_ VMON9_ ABIST2	NOT_ VMON8_ ABIST2
		NOT_ VMON7_ ABIST2	NOT_ VMON6_ ABIST2	NOT_ VMON5_ ABIST2	NOT_ VMON4_ ABIST2	NOT_ VMON3_ ABIST2	NOT_ VMON2_ ABIST2	NOT_ VMON1_ ABIST2	NOT_ VMON0_ ABIST2
	FS_I_WD_CFG	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_IMPACT[1:0]	
		0	0	0	0	0	0	0	0

Table 56. Fail-Safe writing registers overview*...continued*

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	FS_I_NOT_WD_ CFG	NOT_WD_ERR_LIMIT[1:0]		0	NOT_WD_RFR_LIMIT[1:0]		0	NOT_WD_FS_IMPACT[1:0]	
		0	0	0	0	0	0	0	0
	FS_I_SAFE_ INPUTS	FCCU_CFG[2:0]			FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	0	FCCU12_ FS_IMPACT
		FCCU1_ FS_IMPACT	FCCU2_ FS_IMPACT	0	ERRMON_ FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_ FS_IMPACT	0
	FS_I_NOT_SAFE_ INPUTS	NOT_FCCU_CFG[2:0]			NOT_FCCU12_ FLT_POL	NOT_FCCU1_ FLT_POL	NOT_FCCU2_ FLT_POL	0	NOT_FCCU12_ FS_IMPACT
		NOT_FCCU1_ FS_IMPACT	NOT_FCCU2_ FS_IMPACT	0	NOT_ERRMON_ FLT_POL	NOT_ERRMON_ACK_TIME[1:0]		NOT_ERRMON_ FS_IMPACT	0
	FS_I_FSSM	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_IMPACT[1:0]		0	RSTB_DUR	FLASH_ MODE_CFG
		FS0B_SC_ HIGH_CFG	FIRST_DFS_CFG	CLK_MON_DIS	DIS_8S	0	0	0	0
	FS_I_NOT_FSSM	NOT_FLT_ERR_CNT_LIMIT[1:0]		0	NOT_FLT_ERR_IMPACT[1:0]		0	NOT_RSTB_DUR	NOT_FLASH_ MODE_CFG
		NOT_FS0B_ SC_ HIGH_CFG	NOT_FIRST_ DFS_CFG	NOT_CLK_MON_DIS	NOT_DIS_8S	0	0	0	0
	FS_I_SVS1	VMON3_SVS[4:0]					VMON2_SVS[4:2]		
		VMON2_SVS[1:0]		VMON1_SVS[4:0]					0
	FS_I_NOT_SVS1	NOT_VMON3_SVS[4:0]					NOT_VMON2_SVS[4:2]		
		NOT_VMON2_SVS[1:0]		NOT_VMON1_SVS[4:0]					0
	FS_I_SVS2	VMON3_ SVS_ UV_MASK	0	VMON2_ SVS_ UV_MASK	0	VMON1_ SVS_ UV_MASK	0	0	0
		0	0	0	0	0	0	0	0
	FS_I_NOT_SVS2	NOT_VMON3_ SVS_UV_MASK	0	NOT_VMON2_ SVS_UV_MASK	0	NOT_VMON1_ SVS_UV_MASK	0	0	0
		0	0	0	0	0	0	0	0
	FS_WD_ WINDOW_DUR	WDW_PERIOD[4:0]					WDW_DC[2:0]		
		0	0	0	0	WDW_RECOVERY[3:0]			
	FS_NOT_WD_ WINDOW_DUR	NOT_WDW_PERIOD[4:0]					NOT_WDW_DC[2:0]		
		0	0	0	0	NOT_WDW_RECOVERY[3:0]			
	FS_WD_SEED	WD_SEED[15:0]							
	FS_WD_ANSWER	WD_ANSWER[15:0]							

Table 56. Fail-Safe writing registers overview*...continued*

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	FS_OVUVREG_ STATUS1	VMON9_OV	VMON9_UV	VMON8_OV	VMON8_UV	VMON7_OV	VMON7_UV	VMON6_OV	VMON6_UV
		VMON5_OV	VMON5_UV	VMON4_OV	VMON4_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
	FS_OVUVREG_ STATUS2	VMON3_OV	VMON3_UV	0	VMON2_OV	VMON2_UV	0	VMON1_OV	VMON1_UV
		0	VMON0_OV	VMON0_UV	0	0	0	0	0
	FS_SAFE_IOS	PGOOD_DIAG	PGOOD_EVENT	0	EXT_RSTB	0	0	RSTB_EVENT	RSTB_DIAG
		RSTB_REQ	0	0	FS0B_DIAG	FS0B_REQ	GO_TO_INITFS	0	0
	FS_DIAG_SAFETY	FCCU12	FCCU1	FCCU2	ERRMONACK	ERRMON	0	BAD_WD_DATA	BAD_WD_TIMING
		0	0	0	0	0	I2C_FS_CRC	I2C_FS_REQ	0
	FS_INTB_MASK	0	0	INT_INH_VMON9	INT_INH_VMON8	INT_INH_VMON7	INT_INH_VMON6	INT_INH_VMON5	INT_INH_VMON4
		INT_INH_VMON3	INT_INH_VMON2	INT_INH_VMON1	INT_INH_VMON0	INT_INH_ BAD_WD_RFR	INT_INH_ ERRMON	INT_INH_FCCU2	INT_INH_FCCU1
	FS_STATES	0	FS_DBG_EXIT	0	0	OTP_CORRUPT	0	REG_CORRUPT	0
		FS_OTP_EXIT	0	0	0	0	0	0	0

18.2 Fail-safe reading registers overview

Table 57. Fail-safe reading registers overview

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Fail-safe	FS_GRL_FLAGS	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	0	0	0	0
		0	0	0	0	0	0	0	0
	FS_I_OVUV_ SAFE_REACTION1	VMON9_OV_IMPACT[1:0]		VMON9_UV_IMPACT[1:0]		VMON8_OV_IMPACT[1:0]		VMON8_UV_IMPACT[1:0]	
		VMON7_OV_IMPACT[1:0]		VMON7_UV_IMPACT[1:0]		VMON6_OV_IMPACT[1:0]		VMON6_UV_IMPACT[1:0]	
	FS_I_NOT_OVUV_ SAFE_REACTION1	NOT_VMON9_OV_IMPACT[1:0]		NOT_VMON9_UV_IMPACT[1:0]		NOT_VMON8_OV_IMPACT[1:0]		NOT_VMON8_UV_IMPACT[1:0]	
		NOT_VMON7_OV_IMPACT[1:0]		NOT_VMON7_UV_IMPACT[1:0]		NOT_VMON6_OV_IMPACT[1:0]		NOT_VMON6_UV_IMPACT[1:0]	
	FS_I_OVUV_ SAFE_REACTION2	VMON5_OV_IMPACT[1:0]		VMON5_UV_IMPACT[1:0]		VMON4_OV_IMPACT[1:0]		VMON4_UV_IMPACT[1:0]	
		VMON3_OV_IMPACT[1:0]		VMON3_UV_IMPACT[1:0]		VMON2_OV_IMPACT[1:0]		VMON2_UV_IMPACT[1:0]	
	FS_I_NOT_OVUV_ SAFE_REACTION2	NOT_VMON5_OV_IMPACT[1:0]		NOT_VMON5_UV_IMPACT[1:0]		NOT_VMON4_OV_IMPACT[1:0]		NOT_VMON4_UV_IMPACT[1:0]	
		NOT_VMON3_OV_IMPACT[1:0]		NOT_VMON3_UV_IMPACT[1:0]		NOT_VMON2_OV_IMPACT[1:0]		NOT_VMON2_UV_IMPACT[1:0]	
	FS_I_OVUV_ SAFE_REACTION3	VMON1_OV_IMPACT[1:0]		VMON1_UV_IMPACT[1:0]		0	0	0	0
		0	0	0	0	VMON0_OV_IMPACT[1:0]		VMON0_UV_IMPACT[1:0]	
	FS_I_NOT_OVUV_ SAFE_REACTION3	NOT_VMON1_OV_IMPACT[1:0]		NOT_VMON1_UV_IMPACT[1:0]		0	0	0	0
		0	0	0	0	NOT_VMON0_OV_IMPACT[1:0]		NOT_VMON0_UV_IMPACT[1:0]	
	FS_I_VMON_ ABIST2	0	0	0	0	0	0	VMON9_ABIST2	VMON8_ABIST2
		VMON7_ABIST2	VMON6_ABIST2	VMON5_ABIST2	VMON4_ABIST2	VMON3_ABIST2	VMON2_ABIST2	VMON1_ABIST2	VMON0_ABIST2
	FS_I_NOT_VMON_ ABIST2	0	0	0	0	0	0	NOT_ VMON9_ ABIST2	NOT_ VMON8_ ABIST2
		NOT_ VMON7_ ABIST2	NOT_ VMON6_ ABIST2	NOT_ VMON5_ ABIST2	NOT_ VMON4_ ABIST2	NOT_ VMON3_ ABIST2	NOT_ VMON2_ ABIST2	NOT_ VMON1_ ABIST2	NOT_ VMON0_ ABIST2
	FS_I_WD_CFG	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_IMPACT[1:0]	
		0	WD_RFH_CNT[2:0]			WD_ERR_CNT[3:0]			
	FS_I_NOT_WD_ CFG	NOT_WD_ERR_LIMIT[1:0]		0	NOT_WD_RFR_LIMIT[1:0]		0	NOT_WD_FS_IMPACT[1:0]	
		0	0	0	0	0	0	0	0
	FS_I_SAFE_ INPUTS	FCCU_CFG[2:0]			FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	0	FCCU12_ FS_IMPACT
		FCCU1_ FS_IMPACT	FCCU2_ FS_IMPACT	0	ERRMON_ FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_ FS_IMPACT	0
	FS_I_NOT_SAFE_ INPUTS	NOT_FCCU_CFG[2:0]			NOT_FCCU12_ FLT_POL	NOT_FCCU1_ FLT_POL	NOT_FCCU2_ FLT_POL	0	NOT_FCCU12_ FS_IMPACT
		NOT_FCCU1_ FS_IMPACT	NOT_FCCU2_ FS_IMPACT	0	NOT_ERRMON_ FLT_POL	NOT_ERRMON_ACK_TIME[1:0]		NOT_ERRMON_ FS_IMPACT	0

Table 57. Fail-safe reading registers overview*...continued*

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	FS_I_FSSM	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_IMPACT[1:0]		0	RSTB_DUR	FLASH_ MODE_CFG
		FS0B_SC_ HIGH_CFG	FIRST_DFS_CFG	CLK_MON_DIS	DIS_8S	FLT_ERR_CNT[3:0]			
	FS_I_NOT_FSSM	NOT_FLT_ERR_CNT_LIMIT[1:0]		0	NOT_FLT_ERR_IMPACT[1:0]		0	NOT_RSTB_DUR	NOT_FLASH_ MODE_CFG
		NOT_FS0B_ SC_ HIGH_CFG	NOT_FIRST_ DFS_CFG	NOT_CLK_MON_DIS	NOT_DIS_8S	0	0	0	0
	FS_I_SVS1	VMON3_SVS[4:0]					VMON2_SVS[4:2]		
		VMON2_SVS[1:0]		VMON1_SVS[4:0]					0
	FS_I_NOT_SVS1	NOT_VMON3_SVS[4:0]					NOT_VMON2_SVS[4:2]		
		NOT_VMON2_SVS[1:0]		NOT_VMON1_SVS[4:0]					0
	FS_I_SVS2	VMON3_ SVS_ UV_MASK	0	VMON2_ SVS_ UV_MASK	0	VMON1_ SVS_ UV_MASK	0	0	0
		0	0	0	0	0	0	0	0
	FS_I_NOT_SVS2	NOT_VMON3_ SVS_UV_MASK	0	NOT_VMON2_ SVS_UV_MASK	0	NOT_VMON1_ SVS_UV_MASK	0	0	0
		0	0	0	0	0	0	0	0
	FS_WD_ WINDOW_DUR	WDW_PERIOD[4:0]					WDW_DC[2:0]		
		0	0	0	0	WDW_RECOVERY[3:0]			
	FS_NOT_WD_ WINDOW_DUR	NOT_WDW_PERIOD[4:0]					NOT_WDW_DC[2:0]		
		0	0	0	0	NOT_WDW_RECOVERY[3:0]			
	FS_WD_SEED	WD_SEED[15:0]							
	FS_OVUVREG_ STATUS1	VMON9_OV	VMON9_UV	VMON8_OV	VMON8_UV	VMON7_OV	VMON7_UV	VMON6_OV	VMON6_UV
		VMON5_OV	VMON5_UV	VMON4_OV	VMON4_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
	FS_OVUVREG_ STATUS2	VMON3_OV	VMON3_UV	0	VMON2_OV	VMON2_UV	0	VMON1_OV	VMON1_UV
		0	VMON0_OV	VMON0_UV	0	0	0	0	0
	FS_SAFE_IOS	PGOOD_DIAG	PGOOD_EVENT	PGOOD_SNS	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_EVENT	RSTB_DIAG
		0	FS0B_DRV	FS0B_SNS	FS0B_DIAG	0	0	FCCU2_RT	FCCU1_RT
	FS_DIAG_SAFETY	FCCU12	FCCU1	FCCU2	0	ERRMON	ERRMON_STATUS	BAD_WD_DATA	BAD_WD_TIMING
		ABIST1_OK	ABIST2_OK	FCCU12_ERR_RT	FCCU1_ERR_RT	FCCU2_ERR_RT	I2C_FS_CRC	I2C_FS_REQ	LBIST_STATUS
	FS_INTB_MASK	0	0	INT_INH_VMON9	INT_INH_VMON8	INT_INH_VMON7	INT_INH_VMON6	INT_INH_VMON5	INT_INH_VMON4
		INT_INH_VMON3	INT_INH_VMON2	INT_INH_VMON1	INT_INH_VMON0	INT_INH_ BAD_WD_RFR	INT_INH_ ERRMON	INT_INH_FCCU2	INT_INH_FCCU1

Table 57. Fail-safe reading registers overview*...continued*

Logic	Register name	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	FS_STATES	0	0	FS_DBG_MODE_RT	0	OTP_CORRUPT	0	REG_CORRUPT	0
		0	FS_OTP_MODE_RT	0	FSM_STATE				

18.3 FS_GRL_FLAGS register

Table 58. FS_GRL_FLAGS register bit allocation

Bit	15	14	13	12	11	10	9	8
Read	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 59. FS_GRL_FLAGS register bit description

Bit	Symbol	Description	
15	FS_COM_G	Communication error flag (I2C_FS_CRC OR I2C_FS_REQ)	
		0	No error
		1	Communication error detected
		Reset condition: Real-time information - cleared when all individual bits are cleared	
14	FS_WD_G	Watchdog error flag (BAD_WD_DATA OR BAD_WD_TIMING)	
		0	No error
		1	Watchdog error detected
		Reset condition: Real-time information - cleared when all individual bits are cleared	
13	FS_IO_G	IOs error flag (PGOOD_DIAG OR RSTB_DIAG OR FS0B_DIAG)	
		0	No error
		1	IOs error detected
		Reset condition: Real-time information - cleared when all individual bits are cleared	
12	FS_REG_OVUV_G	Monitoring error flag (OR of all VMONx_OV/UV, for x from 0 to 9)	
		0	No error
		1	Over/undervoltage error detected
		Reset condition: Real-time information - cleared when all individual bits are cleared	

18.4 FS_I_OVUV_SAFE_REACTION1 register

Table 60. FS_I_OVUV_SAFE_REACTION1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON9_OV_IMPACT[1:0]		VMON9_UV_IMPACT[1:0]		VMON8_OV_IMPACT[1:0]		VMON8_UV_IMPACT[1:0]	
Read	VMON9_OV_IMPACT[1:0]		VMON9_UV_IMPACT[1:0]		VMON8_OV_IMPACT[1:0]		VMON8_UV_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON7_OV_IMPACT[1:0]		VMON7_UV_IMPACT[1:0]		VMON6_OV_IMPACT[1:0]		VMON6_UV_IMPACT[1:0]	
Read	VMON7_OV_IMPACT[1:0]		VMON7_UV_IMPACT[1:0]		VMON6_OV_IMPACT[1:0]		VMON6_UV_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1

Table 61. FS_I_OVUV_SAFE_REACTION1 register bit description

Bit	Symbol	Description
15 to 14	VMON9_OV_IMPACT[1:0]	See Table 167
13 to 12	VMON9_UV_IMPACT[1:0]	
11 to 10	VMON8_OV_IMPACT[1:0]	
9 to 8	VMON8_UV_IMPACT[1:0]	
7 to 6	VMON7_OV_IMPACT[1:0]	
5 to 4	VMON7_UV_IMPACT[1:0]	
3 to 2	VMON6_OV_IMPACT[1:0]	
1 to 0	VMON6_UV_IMPACT[1:0]	

18.5 FS_I_OVUV_SAFE_REACTION2 register

Table 62. FS_I_OVUV_SAFE_REACTION2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON5_OV_IMPACT[1:0]		VMON5_UV_IMPACT[1:0]		VMON4_OV_IMPACT[1:0]		VMON4_UV_IMPACT[1:0]	
Read	VMON5_OV_IMPACT[1:0]		VMON5_UV_IMPACT[1:0]		VMON4_OV_IMPACT[1:0]		VMON4_UV_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON3_OV_IMPACT[1:0]		VMON3_UV_IMPACT[1:0]		VMON2_OV_IMPACT[1:0]		VMON2_UV_IMPACT[1:0]	
Read	VMON3_OV_IMPACT[1:0]		VMON3_UV_IMPACT[1:0]		VMON2_OV_IMPACT[1:0]		VMON2_UV_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1

Table 63. FS_I_OVUV_SAFE_REACTION2 register bit description

Bit	Symbol	Description
15 to 14	VMON5_OV_IMPACT[1:0]	See Table 167
13 to 12	VMON5_UV_IMPACT[1:0]	
11 to 10	VMON4_OV_IMPACT[1:0]	
9 to 8	VMON4_UV_IMPACT[1:0]	
7 to 6	VMON3_OV_IMPACT[1:0]	
5 to 4	VMON3_UV_IMPACT[1:0]	
3 to 2	VMON2_OV_IMPACT[1:0]	
1 to 0	VMON2_UV_IMPACT[1:0]	

18.6 FS_I_OVUV_SAFE_REACTION3 register

Table 64. FS_I_OVUV_SAFE_REACTION3 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON1_OV_IMPACT[1:0]		VMON1_UV_IMPACT[1:0]		0	0	0	0
Read	VMON1_OV_IMPACT[1:0]		VMON1_UV_IMPACT[1:0]		RESERVED	RESERVED	RESERVED	RESERVED
Reset	1	1	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	VMON0_OV_IMPACT[1:0]		VMON0_UV_IMPACT[1:0]	
Read	RESERVED	RESERVED	RESERVED	RESERVED	VMON0_OV_IMPACT[1:0]		VMON0_UV_IMPACT[1:0]	
Reset	0	0	0	0	1	1	0	1

Table 65. FS_I_OVUV_SAFE_REACTION3 register bit description

Bit	Symbol	Description
15 to 14	VMON1_OV_IMPACT[1:0]	See Table 167
13 to 12	VMON1_UV_IMPACT[1:0]	
3 to 2	VMON0_OV_IMPACT[1:0]	
1 to 0	VMON0_UV_IMPACT[1:0]	

18.7 FS_I_VMON_ABIST2 register

Table 66. FS_I_VMON_ABIST2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	VMON9_ ABIST2	VMON8_ ABIST2
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VMON9_ ABIST2	VMON8_ ABIST2
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON7_ ABIST2	VMON6_ ABIST2	VMON5_ ABIST2	VMON4_ ABIST2	VMON3_ ABIST2	VMON2_ ABIST2	VMON1_ ABIST2	VMON0_ ABIST2
Read	VMON7_ ABIST2	VMON6_ ABIST2	VMON5_ ABIST2	VMON4_ ABIST2	VMON3_ ABIST2	VMON2_ ABIST2	VMON1_ ABIST2	VMON0_ ABIST2
Reset	0	0	0	0	0	0	0	0

Table 67. FS_I_VMON_ABIST2 register bit description

Bit	Symbol	Description	
9	VMON9_ABIST2	VMON9 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON9 after INIT
		Reset condition: POR	
8	VMON8_ABIST2	VMON8 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON8 after INIT
		Reset condition: POR	
7	VMON7_ABIST2	VMON7 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON7 after INIT
		Reset condition: POR	
6	VMON6_ABIST2	VMON6 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON6 after INIT
		Reset condition: POR	
5	VMON5_ABIST2	VMON5 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON5 after INIT
		Reset condition: POR	
4	VMON4_ABIST2	VMON4 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON4 after INIT
		Reset condition: POR	
3	VMON3_ABIST2	VMON3 ABIST2 configuration	
		0	No ABIST

Table 67. FS_I_VMON_ABIST2 register bit description*...continued*

Bit	Symbol	Description	
		1	Run ABIST on VMON3 after INIT
		Reset condition: POR	
2	VMON2_ABIST2	VMON2 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON2 after INIT
		Reset condition: POR	
1	VMON1_ABIST2	VMON1 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON1 after INIT
		Reset condition: POR	
0	VMON0_ABIST2	VMON0 ABIST2 configuration	
		0	No ABIST
		1	Run ABIST on VMON0 after INIT
		Reset condition: POR	

18.8 FS_I_WD_CFG register

Table 68. FS_I_WD_CFG register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_IMPACT[1:0]	
Read	WD_ERR_LIMIT[1:0]		RESERVED	WD_RFR_LIMIT[1:0]		RESERVED	WD_FS_IMPACT[1:0]	
Reset	0	1	0	0	0	0	1	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	RESERVED	WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0

Table 69. FS_I_WD_CFG register bit description

Bit	Symbol	Description	
15 to 14	WD_ERR_LIMIT[1:0]	See Table 151	
12 to 11	WD_RFR_LIMIT[1:0]	See Table 152	
9 to 8	WD_FS_IMPACT[1:0]	See Table 153	
6 to 4	WD_RFR_CNT[2:0]	Reflect the value of the watchdog refresh counter (unsigned integer)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	7
		Reset condition: POR	
3 to 0	WD_ERR_CNT[3:0]	Reflect the value of the watchdog error counter (unsigned integer)	
		0000	0

Table 69. FS_I_WD_CFG register bit description...*continued*

Bit	Symbol	Description	
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		Reset condition: POR	

18.9 FS_I_SAFE_INPUTS register

Table 70. FS_I_SAFE_INPUTS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FCCU_CFG[2:0]			FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	0	FCCU12_ FS_IMPACT
Read	FCCU_CFG[2:0]			FCCU12_ FLT_POL	FCCU1_ FLT_POL	FCCU2_ FLT_POL	RESERVED	FCCU12_ FS_IMPACT
Reset	0	0	1	0	0	0	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	FCCU1_ FS_IMPACT	FCCU2_ FS_IMPACT	0	ERRMON_ FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_ FS_IMPACT	0
Read	FCCU1_ FS_IMPACT	FCCU2_ FS_IMPACT	RESERVED	ERRMON_ FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_ FS_IMPACT	RESERVED
Reset	1	1	0	0	0	1	1	0

Table 71. FS_I_SAFE_INPUTS register bit description

Bit	Symbol	Description
15 to 13	FCCU_CFG[2:0]	See Table 154
12	FCCU12_FLT_POL	See Table 155
11	FCCU1_FLT_POL	See Table 157
10	FCCU2_FLT_POL	See Table 157

Table 71. FS_I_SAFE_INPUTS register bit description*...continued*

Bit	Symbol	Description
8	FCCU12_FS_IMPACT	SeeTable 156
7	FCCU1_FS_IMPACT	See Table 158
6	FCCU2_FS_IMPACT	See Table 158
4	ERRMON_FLT_POL	See Table 170
3 to 2	ERRMON_ACK_TIME[1:0]	See Table 171
1	ERRMON_FS_IMPACT	See Table 172

18.10 FS_I_FSSM register

Table 72. FS_I_FSSM register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_IMPACT[1:0]		0	RSTB_DUR	FLASH_ MODE_CFG
Read	FLT_ERR_CNT_LIMIT[1:0]		RESERVED	FLT_ERR_IMPACT[1:0]		RESERVED	RSTB_DUR	FLASH_ MODE_CFG
Reset	0	1	0	1	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	BACKUP_ SAFETY_PATH	FIRST_ DFS_CFG	CLK_ MON_DIS	DIS_8S	0	0	0	0
Read	BACKUP_ SAFETY_PATH	FIRST_ DFS_CFG	CLK_ MON_DIS	DIS_8S	FLT_ERR_CNT[3:0]			
Reset	1	0	0	OTP	0	0	0	1

Table 73. FS_I_FSSM register bit description

Bit	Symbol	Description	
15 to 14	FLT_ERR_CNT_LIMIT[1:0]	See Table 175	
12 to 11	FLT_ERR_IMPACT[1:0]	See Table 176	
9	RSTB_DUR	RSTB pulse duration configuration	
		0	10 ms
		1	1.0 ms
		Reset condition: POR	
8	FLASH_MODE_CFG	Configure entry in MCU Flash Mode	
		0	Device will not go to MCU Flash Mode
		1	Device will go to MCU Flash Mode
		Reset condition: POR	
7	FS0B_SC_HIGH_CFG	Assert RSTB in case of a short to high detected on FS0B	
		0	RSTB is not asserted
		1	RSTB is asserted
		Reset condition: POR	

Table 73. FS_I_FSSM register bit description*...continued*

Bit	Symbol	Description	
6	FIRST_DFS_CFG	Configure device behavior when FLT_ERR_CNT increment	
		0	No effect
		1	Device will go to DEEP-FS when first FLT_ERR_CNT increment
		Reset condition: POR	
5	CLK_MON_DIS	Disable clock monitoring	
		0	Clock monitoring enabled
		1	Clock monitoring disabled
		Reset condition: POR	
4	DIS_8S	Disable 8 seconds timer	
		0	Device go DEEP-FS if RSTB low longer than 8 seconds
		1	RSTB low timer disabled
		Reset condition: POR	
3 to 0	FLT_ERR_CNT[3:0]	Reflect the value of the fault error counter (unsigned integer)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		1010	10
		1011	11
		1100	12

Table 73. FS_I_FSSM register bit description*...continued*

Bit	Symbol	Description
		Reset condition: Real time information

18.11 FS_I_SVS1 register

Table 74. FS_I_SVS1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON3_SVS[4:0]					VMON2_SVS[4:2]		
Read	VMON3_SVS[4:0]					VMON2_SVS[4:2]		
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON2_SVS[1:0]		VMON1_SVS[4:0]					0
Read	VMON2_SVS[1:0]		VMON1_SVS[4:0]					RESERVED
Reset	0	0	0	0	0	0	0	0

Table 75. FS_I_SVS1 register bit description

Bit	Symbol	Description
15 to 11	VMON3_SVS[4:0]	VMON3 static voltage scaling negative offset (unsigned integer)
		VMON3 SVS offset = VMON3_SVS[4:0] x -6.25 mV (see Table 162)
		Reset condition: POR
10 to 6	VMON2_SVS[4:0]	VMON2 static voltage scaling negative offset (unsigned integer)
		VMON2 SVS offset = VMON2_SVS[4:0] x -6.25 mV (see Table 162)
		Reset condition: POR
5 to 1	VMON1_SVS[4:0]	VMON1 static voltage scaling negative offset (unsigned integer)
		VMON1 SVS offset = VMON1_SVS[4:0] x -6.25 mV (see Table 162)
		Reset condition: POR

18.12 FS_I_SVS2 register

Table 76. FS_I_SVS2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON3_ SVS_ UV_MASK	0	VMON2_ SVS_ UV_MASK	0	VMON1_ SVS_ UV_MASK	0	0	0
Read	VMON3_ SVS_ UV_MASK	REVERVED	VMON2_ SVS_ UV_MASK	REVERVED	VMON1_ SVS_ UV_MASK	REVERVED	REVERVED	REVERVED
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	0	0	0	0
Read	REVERVED	REVERVED	REVERVED	REVERVED	REVERVED	REVERVED	REVERVED	REVERVED
Reset	0	0	0	0	0	0	0	0

Table 77. FS_I_SVS2 register bit description

Bit	Symbol	Description	
15	VMON3_SVS_UV_MASK	VMON3 Static Voltage Scaling UV mask	
		0	Do not mask VMON3 UV impact
		1	Mask VMON3 UV impact during SVS procedure (UV flag active)
		Reset condition: POR and NOT INIT_FS	
13	VMON2_SVS_UV_MASK	VMON2 Static Voltage Scaling UV mask	
		0	Do not mask VMON2 UV impact
		1	Mask VMON2 UV impact during SVS procedure (UV flag active)
		Reset condition: POR and NOT INIT_FS	
11	VMON1_SVS_UV_MASK	VMON1 Static Voltage Scaling UV mask	
		0	Do not mask VMON1 UV impact
		1	Mask VMON1 UV impact during SVS procedure (UV flag active)
		Reset condition: POR and NOT INIT_FS	

18.13 FS_WD_WINDOW register

Table 78. FS_WD_WINDOW register bit

Bit	15	14	13	12	11	10	9	8
Write	WDW_PERIOD[4:0]					WDW_DC[2:0]		
Read	WDW_PERIOD[4:0]					WDW_DC[2:0]		
Reset	0	0	0	1	1	0	1	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	0	0	0	WDW_RECOVERY[3:0]			
Read	RESERVED	RESERVED	RESERVED	RESERVED	WDW_RECOVERY [3:0]			
Reset	0	0	0	0	1	0	1	1

Table 79. FS_WD_WINDOW register bit description

Bit	Symbol	Description
15 to 11	WDW_PERIOD[4:0]	See Table 148
10 to 8	WDW_DC[2:0]	See Table 149
3 to 0	WDW_RECOVERY[3:0]	See Table 154

18.14 FS_WD_SEED register

Table 80. FS_WD_SEED register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	WD_SEED[15:0]															
Read	WD_SEED[15:0]															
Reset	0	1	0	1	1	0	1	0	1	0	1	1	0	0	1	0

Table 81. FS_WD_ANSWER register bit description

Bit	Symbol	Description
15 to 0	WD_SEED[15:0]	Watchdog seed value

Table 81. FS_WD_ANSWER register bit description...*continued*

Bit	Symbol	Description
		0x5AB2 default value at startup
		Reset condition: POR

18.15 FS_WD_ANSWER register

Table 82. FS_WD_ANSWER register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	WD_ANSWER[15:0]															

Table 83. Table 98. FS_WD_ANSWER register bit description

Bit	Symbol	Description
15 to 0	WD_ANSWER[15:0]	Watchdog valid answer value from the MCU
		Challenger WD: WD_ANSWER = (NOT(((WD_SEED x 4)+6)–4))/4 see Section 31.4.1.2 "Challenger Watchdog"
		Simple WD: WD_ANSWER = WD_SEED see Section 31.4.1.1 "Simple Watchdog"

18.16 FS_OVUVREG_STATUS1 register

Table 84. FS_OVUVREG_STATUS1 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON9_OV	VMON9_UV	VMON8_OV	VMON8_UV	VMON7_OV	VMON7_UV	VMON6_OV	VMON6_UV
Read	VMON9_OV	VMON9_UV	VMON8_OV	VMON8_UV	VMON7_OV	VMON7_UV	VMON6_OV	VMON6_UV
Reset	0	1	0	1	0	1	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	VMON5_OV	VMON5_UV	VMON4_OV	VMON4_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
Read	VMON5_OV	VMON5_UV	VMON4_OV	VMON4_UV	RESERVED	FS_DIG_REF_OV	FS_OSC_DRIFT	RESERVED
Reset	0	1	0	1	0	0	0	0

Table 85. Table 100. FS_OVUVREG_STATUS1 register bit description

Bit	Symbol	Description	
15	VMON9_OV	Overvoltage Monitoring on VMON9	
		0	No event
		1	Overvoltage reported on VMON9
		Reset condition: POR / clear on write (write ‘1’)	
14	VMON9_UV	Undervoltage Monitoring on VMON9	
		0	No event
		1	Undervoltage reported on VMON9
		Reset condition: POR / clear on write (write ‘1’)	
13	VMON8_OV	Overvoltage Monitoring on VMON8	
		0	No event
		1	Overvoltage reported on VMON8
		Reset condition: POR / clear on write (write ‘1’)	
12	VMON8_UV	Undervoltage Monitoring on VMON8	
		0	No event
		1	Undervoltage reported on VMON8
		Reset condition: POR / clear on write (write ‘1’)	
11	VMON7_OV	Overvoltage Monitoring on VMON7	
		0	No event
		1	Overvoltage reported on VMON7
		Reset condition: POR / clear on write (write ‘1’)	
10	VMON7_UV	Undervoltage Monitoring on VMON7	
		0	No event
		1	Undervoltage reported on VMON7
		Reset condition: POR / clear on write (write ‘1’)	
9	VMON6_OV	Overvoltage Monitoring on VMON6	
		0	No event

Table 85. Table 100. FS_OVUVREG_STATUS1 register bit description*...continued*

Bit	Symbol	Description	
		1	Overvoltage reported on VMON6
		Reset condition: POR / clear on write (write ‘1’)	
8	VMON6_UV	Undervoltage Monitoring on VMON6	
		0	No event
		1	Undervoltage reported on VMON6
		Reset condition: POR / clear on write (write ‘1’)	
7	VMON5_OV	Overvoltage Monitoring on VMON5	
		0	No event
		1	Overvoltage reported on VMON5
		Reset condition: POR / clear on write (write ‘1’)	
6	VMON5_UV	Undervoltage Monitoring on VMON5	
		0	No event
		1	Undervoltage reported on VMON5
		Reset condition: POR / clear on write (write ‘1’)	
5	VMON4_OV	Overvoltage Monitoring on VMON4	
		0	No event
		1	Overvoltage reported on VMON4
		Reset condition: POR / clear on write (write ‘1’)	
4	VMON4_UV	Undervoltage Monitoring on VMON4	
		0	No event
		1	Undervoltage reported on VMON4
		Reset condition: POR / clear on write (write ‘1’)	
2	FS_DIG_REF_OV	Overvoltage of the internal digital fail-safe reference voltage	
		0	No overvoltage
		1	Overvoltage reported of the internal digital fail-safe reference voltage
		Reset condition: POR / clear on write (write ‘1’)	

Table 85. Table 100. FS_OVUVREG_STATUS1 register bit description*...continued*

Bit	Symbol	Description	
1	FS_OSC_DRIFT	Drift of the fail-safe OSC	
		0	No drift
		1	Oscillator drift
		Reset condition: POR / clear on write (write '1')	

18.17 FS_OVUVREG_STATUS2 register

Table 86. FS_OVUVREG_STATUS2 register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	VMON3_OV	VMON3_UV	0	VMON2_OV	VMON2_UV	0	VMON1_OV	VMON1_UV
Read	VMON3_OV	VMON3_UV	RESERVED	VMON2_OV	VMON2_UV	RESERVED	VMON1_OV	VMON1_UV
Reset	0	1	0	0	1	0	0	1
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	0	VMON0_OV	VMON0_UV	0	0	0	0	0
Read	RESERVED	VMON0_OV	VMON0_UV	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	1	0	0	0	0	0

Table 87. FS_OVUVREG_STATUS2 register bit description

Bit	Symbol	Description	
15	VMON3_OV	Overvoltage Monitoring on VMON3	
		0	No event
		1	Overvoltage reported on VMON3
		Reset condition: POR / clear on write (write '1')	
14	VMON3_UV	Undervoltage Monitoring on VMON3	
		0	No event
		1	Undervoltage reported on VMON3

Table 87. FS_OVUVREG_STATUS2 register bit description *...continued*

Bit	Symbol	Description	
		Reset condition: POR / clear on write (write ‘1’)	
12	VMON2_OV	Overvoltage Monitoring on VMON2	
		0	No event
		1	Overvoltage reported on VMON2
		Reset condition: POR / clear on write (write ‘1’)	
11	VMON2_UV	Undervoltage Monitoring on VMON2	
		0	No event
		1	Undervoltage reported on VMON2
		Reset condition: POR / clear on write (write ‘1’)	
9	VMON1_OV	Overvoltage Monitoring on VMON1	
		0	No event
		1	Overvoltage reported on VMON1
		Reset condition: POR / clear on write (write ‘1’)	
8	VMON1_UV	Undervoltage Monitoring on VMON1	
		0	No event
		1	Undervoltage reported on VMON1
		Reset condition: POR / clear on write (write ‘1’)	
6	VMON0_OV	Overvoltage Monitoring on VMON0	
		0	No event
		1	Overvoltage reported on VMON0
		Reset condition: POR / clear on write (write ‘1’)	
5	VMON0_UV	Undervoltage Monitoring on VMON0	
		0	No event
		1	Undervoltage reported on VMON0
		Reset condition: POR / clear on write (write ‘1’)	

18.18 FS_RELEASE_FS0B register

Table 88. FS_RELEASE_FS0B register bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	RELEASE_FS0B[15:0]															

Table 89. FS_RELEASE_FS0B register bit description

Bit	Symbol	Description
15 to 0	RELEASE_FS0B [15:0]	Secure 16-bits word to release FS0B
		Depend on WD_SEED value and calculation. See Section 31.9.4 "FS0B release"

18.19 FS_SAFE_IOs register

Table 90. FS_SAFE_IOS register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	PGOOD_DIAG	PGOOD_EVENT	0	EXT_RSTB	0	0	RSTB_EVENT	RSTB_DIAG
Read	PGOOD_DIAG	PGOOD_EVENT	PGOOD_SNS	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_EVENT	RSTB_DIAG
Reset	0	1	0	0	1	1	1	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	RSTB_REQ	0	0	FS0B_DIAG	FS0B_REQ	GO_TO_INITFS	0	0
Read	RESERVED	FS0B_DRV	FS0B_SNS	FS0B_DIAG	RESERVED	RESERVED	FCCU2_RT	FCCU1_RT
Reset	0	0	0	0	0	0	0	1

Table 91. FS_SAFE_IOS register bit description

Bit	Symbol	Description	
15	PGOOD_DIAG	Report a PGOOD Short to High	
		0	No failure
		1	Short circuit HIGH
		Reset condition: POR / clear on write (write ‘1’)	
14	PGOOD_EVENT	Report a Power GOOD event	

Table 91. FS_SAFE_IOS register bit description*...continued*

Bit	Symbol	Description	
		0	No event
		1	Power GOOD event occurred
		Reset condition: POR / clear on write (write ‘1’)	
13	PGOOD_SNS	Sense of PGOOD pad	
		0	PGOOD pad sensed low
		1	PGOOD pad sensed high
		Reset condition: Real time information	
12	EXT_RSTB	Report an external RESET	
		0	No event
		1	External RESET
		Reset condition: POR / clear on write (write ‘1’)	
11	RSTB_DRV	RSTB driver – digital command	
		0	RSTB driver command sensed low
		1	RSTB driver command sensed high
		Reset condition: Real time information	
10	RSTB_SNS	Sense of RSTB pad	
		0	RSTB pad sensed low
		1	RSTB pad sensed high
		Reset condition: Real time information	
9	RSTB_EVENT	Report a RSTB event	
		0	No event
		1	RESET occurred
		Reset condition: POR / clear on write (write ‘1’)	
8	RSTB_DIAG	Report a RSTB short to high	
		0	No failure
		1	Short circuit high

Table 91. FS_SAFE_IOS register bit description*...continued*

Bit	Symbol	Description	
		Reset condition: POR / clear on write (write '1')	
7	RSTB_REQ	Request assertion of RSTB (Pulse)	
		0	No event
		1	RSTB assertion required (pulse)
		Reset condition: POR	
6	FS0B_DRV	FS0B driver – digital command	
		0	FS0B driver command sensed low
		1	FS0B driver command sensed high
		Reset condition: Real time information	
5	FS0B_SNS	Sense of FS0B pad	
		0	FS0B pad sensed low
		1	FS0B pad sensed high
		Reset condition: Real time information	
4	FS0B_DIAG	Report a failure on FS0B	
		0	No event
		1	Short circuit high
		Reset condition: POR / clear on write (write '1')	
3	FS0B_REQ	Request assertion of FS0B	
		0	No assertion
		1	FS0B assertion
		Reset condition: POR	
2	GO_TO_INITFS	Go back to INIT fail-safe request	
		0	No action
		1	Go back to INIT_FS
		Reset condition: POR	
1	FCCU2_RT	Report FCCU2 pin level	

Table 91. FS_SAFE_IOS register bit description*...continued*

Bit	Symbol	Description	
		0	LOW level
		1	HIGH level
		Reset condition: Real time information	
0	FCCU1_RT	Report FCCU1 pin level	
		0	LOW level
		1	HIGH level
		Reset condition: Real time information	

18.20 FS_DIAG_SAFETY register

Table 92. FS_DIAG_SAFETY register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	FCCU12	FCCU1	FCCU2	ERRMONACK	ERRMON	0	BAD_WD_ DATA	BAD_WD_ TIMING
Read	FCCU12	FCCU1	FCCU2	RESERVED	ERRMON	ERRMON_ STATUS	BAD_WD_ DATA	BAD_WD_ TIMING
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	0	0	0	0	0	I2C_FS_CRC	I2C_FS_REQ	0
Read	ABIST1_OK	ABIST2_OK	FCCU12_ERR_RT	FCCU1_ERR_RT	FCCU2_ERR_RT	I2C_FS_CRC	I2C_FS_REQ	LBIST_OK
Reset	1	0	0	0	0	0	0	1

Table 93. FS_DIAG_SAFETY register bit description

Bit	Symbol	Description	
15	FCCU12	Report an error in the FCCU12 input	
		0	No error
		1	Error detected
		Reset condition: POR / clear on write (write '1')	
14	FCCU1	Report an error in the FCCU1 input	
		0	No error

Table 93. FS_DIAG_SAFETY register bit description*...continued*

Bit	Symbol	Description	
		1	Error detected
		Reset condition: POR / clear on write (write '1')	
13	FCCU2	Report an error in the FCCU2 input	
		0	No error
		1	Error detected
		Reset condition: POR / clear on write (write '1')	
12	ERRMONACK	Acknowledge ERRMON failure detection from MCU	
		0	No effect
		1	Acknowledge ERRMON failure detection
		Reset condition: POR	
11	ERRMON	Report an error in the ERRMON input	
		0	No error
		1	Error detected
		Reset condition: POR / clear on write (write '1')	
10	ERRMON_STATUS	Report ERRMON pin level	
		0	LOW level
		1	HIGH level
		Reset condition: Real time information	
9	BAD_WD_DATA	WD refresh status - Data	
		0	Good WD refresh
		1	Bad WD refresh, error in the DATA
		Reset condition: POR / clear on write (write '1')	
8	BAD_WD_TIMING	WD refresh status - Timing	
		0	Good WD refresh
		1	Bad WD refresh, wrong window or in timeout
		Reset condition: POR / clear on write (write '1')	

Table 93. FS_DIAG_SAFETY register bit description*...continued*

Bit	Symbol	Description	
7	ABIST1_OK	Diagnostic of Analog BIST1	
		0	ABIST1 FAIL
		1	ABIST1 PASS
		Reset condition: Real time information	
6	ABIST2_OK	Diagnostic of Analog BIST2	
		0	ABIST2 FAIL or NOT EXECUTED
		1	ABIST2 PASS
		Reset condition: Real time information	
5	FCCU12_ERR_RT	Real time Diagnostic of FCCU12 detection	
		0	No error
		1	Error on FCCU12 detected
		Reset condition: POR / clear on write (write ‘1’)	
4	FCCU1_ERR_RT	Real time Diagnostic of FCCU1 detection	
		0	No error
		1	Error on FCCU1 detected
		Reset condition: POR / clear on write (write ‘1’)	
3	FCCU2_ERR_RT	Real time Diagnostic of FCCU2 detection	
		0	No error
		1	Error on FCCU2 detected
		Reset condition: POR / clear on write (write ‘1’)	
2	I2C_FS_CRC	Fail-safe I2C communication CRC issue	
		0	No error
		1	Error detected in the CRC
		Reset condition: POR / clear on write (write ‘1’)	
1	I2C_FS_REQ	Invalid fail-safe I2C access (wrong write or read, write to INIT registers in normal mode, wrong address)	
		0	No error

Table 93. FS_DIAG_SAFETY register bit description*...continued*

Bit	Symbol	Description	
		1	I2C violation
		Reset condition: POR / clear on write (write '1')	
0	LBIST_OK	Diagnostic of Logical BIST	
		0	LBIST FAIL
		1	LBIST PASS
		Reset condition: Real time information	

18.21 FS_INTB_MASK register

Table 94. FS_INTB_MASK register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	0	INT_INH_ VMON9	INT_INH_ VMON8	INT_INH_ VMON7	INT_INH_ VMON6	INT_INH_ VMON5	INT_INH_ VMON4
Read	RESERVED	RESERVED	INT_INH_ VMON9	INT_INH_ VMON8	INT_INH_ VMON7	INT_INH_ VMON6	INT_INH_ VMON5	INT_INH_ VMON4
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	INT_INH_ VMON3	INT_INH_ VMON2	INT_INH_ VMON1	INT_INH_ VMON0	INT_INH_ BAD_WD_ REFRESH	INT_INH_ ERRMON	INT_INH_ FCCU2	INT_INH_ FCCU1
Read	INT_INH_ VMON3	INT_INH_ VMON2	INT_INH_ VMON1	INT_INH_ VMON0	INT_INH_ BAD_WD_ REFRESH	INT_INH_ ERRMON	INT_INH_ FCCU2	INT_INH_ FCCU1
Reset	0	0	0	0	0	0	0	0

Table 95. FS_INTB_MASK register bit description

Bit	Symbol	Description	
13	INT_INH_VMON9	Inhibit INTERRUPT on VMON9 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
12	INT_INH_VMON8	Inhibit INTERRUPT on VMON8 OV and UV event	
		0	Interruption NOT MASKED

Table 95. FS_INTB_MASK register bit description*...continued*

Bit	Symbol	Description	
		1	Interruption MASKED
		Reset condition: POR	
11	INT_INH_VMON7	Inhibit INTERRUPT on VMON7 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
10	INT_INH_VMON6	Inhibit INTERRUPT on VMON6 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
9	INT_INH_VMON5	Inhibit INTERRUPT on VMON5 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
8	INT_INH_VMON4	Inhibit INTERRUPT on VMON4 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
7	INT_INH_VMON3_OV_UV	Inhibit INTERRUPT on VMON3 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
6	INT_INH_VMON2_OV_UV	Inhibit INTERRUPT on VMON2 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	

Table 95. FS_INTB_MASK register bit description...*continued*

Bit	Symbol	Description	
5	INT_INH_VMON1_OV_UV	Inhibit INTERRUPT on VMON1 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
4	INT_INH_VMON0_OV_UV	Inhibit INTERRUPT on VMON0 OV and UV event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
3	INT_INH_BAD_WD_REFRESH	Inhibit INTERRUPT on bad WD refresh event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
2	INT_INH_ERRMON	Inhibit INTERRUPT on ERRMON event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
1	INT_INH_FCCU2	Inhibit INTERRUPT on FCCU2 event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	
0	INT_INH_FCCU1	Inhibit INTERRUPT on FCCU1 event	
		0	Interruption NOT MASKED
		1	Interruption MASKED
		Reset condition: POR	

18.22 FS_STATES register

Table 96. FS_STATES register bit allocation

Bit	15	14	13	12	11	10	9	8
Write	0	FS_DBG_EXIT	0	0	OTP_CORRUPT	0	REG_CORRUPT	0
Read	RESERVED	RESERVED	FS_DBG_ MODE_RT	RESERVED	OTP_CORRUPT	RESERVED	REG_CORRUPT	RESERVED
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Write	FS_OTP_EXIT	0	0	0	0	0	0	0
Read	RESERVED	FS_OTP_ MODE_RT	RESERVED	FSM_STATE[4:0]				
Reset	0	0	0	0	0	1	1	0

Table 97. FS_STATES register bit description

Bit	Symbol	Description	
14	FS_DBG_EXIT	Leave FS_DEBUG mode	
		0	No action
		1	Leave DEBUG mode
		Reset condition: POR	
13	FS_DBG_MODE_RT	Real time FS_DEBUG mode status	
		0	NOT in DEBUG mode
		1	In DEBUG mode
		Reset condition: Real time information	
11	OTP_CORRUPT	OTP bits corruption detection (5 ms cyclic check)	
		0	No error
		1	OTP CRC error detected
		Reset condition: POR / clear on write (write ‘1’)	
9	REG_CORRUPT	INIT register corruption detection (real time comparison between FS_I_REGISTER/FS_I_NOT_REGISTER)	
		0	No error
		1	INIT register content mismatch detected

Table 97. FS_STATES register bit description*...continued*

		Reset condition: POR / clear on write (write ‘1’)	
8	FS_OTP_EXIT	Leave FS_OTP mode	
		0	No action
		1	Leave OTP mode
		Reset condition: POR	
6	FS_OTP_MODE_RT	Real time FS_OTP mode status	
		0	NOT in OTP mode
		1	In OTP mode
		Reset condition: Real time information	
4 to 0	FSM_STATE[3:0]	Report fail-safe state machine current state	
		00000	FS3 – LOAD FUSE
		00001	FS4 – FS OTP MODE
		00010	FS5 – FS READY
		00011	FS6 – WAIT ABIST1
		00100	FS7 – ABIST1
		00101	FS8 – RELEASE RSTB
		00110	FS9 – INIT_FS
		00111	FS10 – WAIT ABIST2
		01000	FS11 – ABSIT2
		01001	FS12 – ASSERT FS0B
		01010	FS13 – NORMAL_FS
		01011	FS14 – ASSERT RSTB
		01100	FS15 – ASSERT PGOOD
		01101	FS91 – FLASH MODE
		Reset condition: Real time information	

19 OTP bits description

19.1 Main OTP Overview

Table 98. Main OTP_REGISTERS

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OTP_CFG_ VPRE_1	0x0C	VPRETON[1:0]		VPREV[5:0]					
OTP_CFG_ VPRE_2	0x0D	0	VPRESSR AMP	VPRESC[5:0]					
OTP_CFG_ VPRE_3	0x0E	VPREILIM[1:0]		VPRETOFF[1:0]		**VPRESRLS[1:0]**[1]		**VPRESRHS[1:0]**[1]	
OTP_CFG_ BOOST_1	0x0F	VBOOSTS[3:0]				BOOSTV[3:0]			
OTP_CFG_ BOOST_2	0x10	BOOSTEN	BOOSTONTIME[1:0]		BOOSTSC[4:0]				
OTP_CFG_ BOOST_3	0x11	BOOSTRCOMP[1:0]		BOOSTCCOMP[1:0]		BOOSTILIM[1:0]		**BOOSTSR[1:0]**	
OTP_CFG_ LVBUCK_1	0x12	BUCKEN	BUCKINDOPT[1:0]		BUCKV[4:0]				
OTP_CFG_ LVBUCK_2	0x13	0	BUCK_PH[2:0]			BUCK_ CTRL_RC	BUCK_ CTRL_GM	BUCKILIM[1:0]	
OTP_CFG_ LVBUCK_3	0x14	BUCK_DVS[1:0]		TSLOT[1:0]		BUCKS[3:0]			
OTP_CFG_ LDO1	0x15	LDO1V[3:0]				LDO1S[3:0]			
OTP_CFG_ LDO2	0x16	LDO2ILIM	LDO2V[2:0]			LDO2S[3:0]			
OTP_CFG_ CLOCK_1	0x17	VPRE_ CLK_SEL	VPRE_PH[2:0]			BOOST_ CLK_SEL	BOOST_PH[2:0]		
OTP_CFG_ CLOCK_2	0x18	**MOD_ CONF**[1]	**MOD_EN**[1]	CLK_DIV2[2:0]			CLK_DIV1[1:0]		PLL_SEL
OTP_CFG_ FSYNC	0x19	0	0	0	FOUT_ SLOT_EN	**FOUTS[3:0]**[1]			
OTP_CFG_ XFAILB	0x1A	0	XFAILB_ PWD_CFG	XFAILB_CFG[1:0]		**XFAILBS[3:0]**[1]			
OTP_CFG_ PWRUP	0x1B	PWRUP_LASTS[3:0]				PWRDWN_FIRSTS[3:0]			
OTP_CFG_ TSD	0x1C	0	0	0	0	**CONF_TSD_ BOOST**[1]	**CONF_TSD_ BUCK**[1]	**CONF_TSD_ LDO1**[1]	**CONF_TSD_ LDO2**[1]
OTP_CFG_ SYS	0x1D	PWRDWN_ DFS	LDO1_ SW_EN	TBAT_ SW_CFG	BAT_SW_EN	VSUP_CFG	VPRE_ OFF_DLY	AUTORETRY_INFINITE	AUTORETRY_EN
OTP_CFG_ VMON	0x1E	0	0	**VMON1_REG_ASSIGN[2:0]**[1]			**VMON0_REG_ASSIGN[2:0]**[1]		
OTP_CFG_I2C	0x1F	0	**VMON4_REG_ASSIGN[2:0]**[1]			I2CDEVADDR[3:0]			
OTP_CFG_ DEVID	0x20	DeviceID[7:0]							

[1] OTP bits can be changed later by I^2C.

19.2 Main OTP bit description

Table 99. OTP_CFG_VPRE_1 register bit description

Address	Register	Bit	Symbol	Value	Description
0x0C	OTP_CFG_ VPRE_1	7 to 6	VPRETON[1:0]		Minimum ON Time
				01	65 ns @ F_{PRE_SW} = 455 kHz
				10	25 ns @ F_{PRE_SW} = 2.22 MHz
		5 to 0	VPREV[5:0]		VPRE output voltage
				001111	3.3 V
				010000	3.4 V
				010001	3.5 V
				010010	3.6 V
				010011	3.7 V
				010100	3.8 V
				010101	3.9 V
				010110	4.0 V
				010111	4.1 V
				011000	4.2 V
				011001	4.3 V
				011010	4.4 V
				011011	4.5 V
				011100	4.6 V
				011101	4.7 V
				011110	4.8 V
				011111	4.9 V
				100000	5.0 V

Table 100. OTP_CFG_VPRE_2 register bit description

Address	Register	Bit	Symbol	Value	Description
0x0D	OTP_CFG_ VPRE_2	6	VPRESSRAMP		VPRE soft start time
				0	1.0 ms
				1	0.5 ms
		5 to 0	VPRESC[5:0]		VPRE slope compensation
				000010	21 mV/us
				000011	31 mV/us
				000100	41 mV/us
				000101	52 mV/us
				000110	62 mV/us

Table 100. OTP_CFG_VPRE_2 register bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
				000111	73 mV/us
				001000	83 mV/us
				001001	93 mV/us
				001010	103 mV/us
				001011	114 mV/us
				001100	124 mV/us
				001101	134 mV/us
				001110	145 mV/us
				001111	155 mV/us
				010000	175 mV/us
				010001	196 mV/us
				010010	217 mV/us
				010011	237 mV/us
				010100	258 mV/us
				010101	279 mV/us
				010110	299 mV/us
				010111	320 mV/us
				011000	340 mV/us
				011001	361 mV/us
				011010	381 mV/us
				011011	402 mV/us
				011100	423 mV/us
				011101	444 mV/us
				011110	464 mV/us
				011111	485 mV/us
				100000	504 mV/us

Table 101. OTP_CFG_VPRE_3 register bit description

Address	Register	Bit	Symbol	Value	Description
0x0E	OTP_CFG_ VPRE_3	7 to 6	VPREILIM[1:0]		VPRE current sense limitation threshold
				00	50 mV
				01	80 mV
				10	120 mV
				11	150 mV
		5 to 4	VPRETOFF[1:0]		VPRE minimum OFF time value
				00	80 ns

Table 101. OTP_CFG_VPRE_3 register bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
		3 to 2	VPRESRLS[1:0]		VPRE low-side driver current control (slew-rate)
				11	PU/PD/900 mA
		1 to 0	VPRESRHS[1:0]		VPRE high-side driver current control (slew-rate)
				00	PU/PD/130 mA
				01	PU/PD/260 mA
				10	PU/PD/520 mA
				11	PU/PD/900 mA

Table 102. OTP_CFG_BOOST_1 register bit description

Address	Register	Bit	Symbol	Value	Description
0x0F	OTP_CFG_BOOST_1	5 to 3	BOOSTS[3:0]		BOOST sequencing turn-ON/OFF slot
					See Table 8
		3 to 0	BOOSTV[3:0]		BOOST output voltage
				0110	5.00 V
				0111	5.09 V
				1000	5.19 V
				1001	5.29 V
				1010	5.40 V
				1011	5.51 V
				1100	5.63 V
				1101	5.74 V
				1110	5.87 V
				1111	6.00 V

Table 103. OTP_CFG_BOOST_2 register bit description

Address	Register	Bit	Symbol	Value	Description
0x10	OTP_CFG_BOOST_2	7	BOOSTEN		BOOST enable
				0	Disabled
				1	Enabled
		6 to 5	BOOSTONTIME[1:0]		BOOST minimum ON time
				00	60 ns
				01	50 ns
				10	70 ns
				11	80 ns

Table 103. OTP_CFG_BOOST_2 register bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
		4 to 0	BOOSTSC[4:0]		BOOST slope compensation
				00010	358 mV/µs
				01001	315 mV/µs
				00100	257 mV/µs
				00011	253 mV/µs
				00101	198 mV/µs
				01010	178 mV/µs
				00110	160 mV/µs
				11001	155 mV/µs
				00111	135 mV/µs
				01100	125 mV/µs
				01101	98 mV/µs
				11010	90 mV/µs
				01110	79 mV/µs
				01111	67 mV/µs
				11100	64 mV/µs
				11101	49 mV/µs
				11110	40 mV/µs
				11111	33 mV/µs

Table 104. OTP_CFG_BOOST_3 register bit description

Address	Register	Bit	Symbol	Value	Description
0x11	OTP_CFG_BOOST_3	7 to 6	BOOSTRCOMP[1:0]		BOOST resistor compensation R_{COMP}
				00	750 kΩ
				01	500 kΩ
		5 to 4	BOOSTCCOMP[1:0]		BOOST capacitor compensation C_{COMP}
				00	125 pF
		3 to 2	BOOSTILIM[1:0]		BOOST LS/inductor peak current limitation
				01	2 A
				10	3 A
		1 to 0	BOOSTSR[1:0]		BOOST low-side slew rate control
				00	50 V/µs
				01	100 V/µs
				10	300 V/µs
				11	500 V/µs

Table 105. OTP_CFG_LVBUCK_1 register bit description

Address	Register	Bit	Symbol	Value	Description
0x12	OTP_CFG_ LVBUCK_1	7	BUCKEN		BUCK enable
				0	Disabled
				1	Enabled
		6 to 5	BUCKINDOPT[1:0]		BUCK inductor selection
				00	1.0 µH
				01	0.47 µH
				10	1.5 µH
		4 to 0	BUCKV[4:0]		BUCK output voltage
				00000	1.0 V
				00001	1.1 V
				00010	1.2 V
				00011	1.25 V
				00100	1.3 V
				00101	1.35 V
				00110	1.5 V
				00111	1.6 V
				01000	1.8 V
				01001	1.85 V
				01010	2.0 V
				01011	2.1 V
				01000	2.15 V
				01001	2.25 V
				01110	2.3 V
				01111	2.4 V
				10000	2.5 V
				10001	2.8 V
				10010	3.15 V
				10011	3.2 V
				10100	3.25 V
				10101	3.3 V

Table 106. OTP_CFG_LVBUCK_2 register bit description

Address	Register	Bit	Symbol	Value	Description
0x13	OTP_CFG_ LVBUCK_2	7	BUCK_CLK_SEL		BUCK clock selection
				0	BUCK_clk = CLK1 (2.22 MHz typical)
		6 to 4	BUCK_PH[2:0]		BUCK phase (delay) selection

Table 106. OTP_CFG_LVBUCK_2 register bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
					See Table 142
		3	BUCK_CTRL_RC		BUCK compensation resistance
				0	65 kΩ
		2	BUCK_CTRL_GM		BUCK amplifier transconductance
				0	48 µS (V_{BUCK} <= 2.0 V)
				0	64 µS (V_{BUCK} > 2.0 V)
		1 to 0	BUCKILIM[1:0]		BUCK current limitation
				01	2.1 A
				11	4.5 A

Table 107. OTP_CFG_LVBUCK_3 register bit description

Address	Register	Bit	Symbol	Value	Description
0x14	OTP_CFG_LVBUCK_3	7 to 6	BUCK_DVS[1:0]		BUCK soft start/stop configurability
				00	10.4 mV/µs
				01	3.5 mV/µs
				10	2.6 mV/µs
				11	2.1 mV/µs
		5 to 4	TSLOT		Power up/down slot duration
				00	0.5 ms
				01	1.0 ms
				10	2.0 ms
				11	8.0 ms
		3 to 0	BUCKS[3:0]		BUCK sequencing turn-ON/OFF slot
					See Table 8

Table 108. OTP_CFG_LDO1 register bit description

Address	Register	Bit	Symbol	Value	Description
0x15	OTP_CFG_LDO1	7 to 4	LDO1V[3:0]		LDO1 output voltage
				0000	1.5 V
				0001	1.6 V
				0010	1.8 V
				0011	1.85 V
				0100	2.15 V
				0101	2.5 V
				0110	2.8 V

Table 108. OTP_CFG_LDO1 register bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
				0111	3.0 V
				1000	3.1 V
				1001	3.15 V
				1010	3.2 V
				1011	3.3 V
				1100	3.35 V
				1101	4.0 V
				1110	4.9 V
				1111	5.0 V
		3 to 0	LDO1S[3:0]		LDO1 sequencing turn-ON/OFF slot
					See Table 8

Table 109. OTP_CFG_LDO2 register bit description

Address	Register	Bit	Symbol	Value	Description
0x16	OTP_CFG_ LDO2	7	LDO2ILIM		LDO2 current limitation
				0	400 mA
				1	150 mA
		6 to 4	LDO2V[2:0]		LDO2 output voltage
				000	1.1 V
				001	1.2 V
				010	1.6 V
				011	1.8 V
				100	2.5 V
				101	2.8 V
				110	3.3 V
				111	5.0 V
		3 to 0	LDO2S[3:0]		LDO2 sequencing turn-ON/OFF slot
					See Table 8

Table 110. OTP_CFG_CLOCK_1 register bit description

Address	Register	Bit	Symbol	Value	Description
0x17	OTP_CFG_ CLOCK_1	7	VPRE_CLK_SEL		VPRE clock selection
				0	VPRE_clk = CLK1 (2.22 MHz typical)
				1	VPRE_clk = CLK2 (455 kHz typical)
		6 to 4	VPRE_PH[2:0]		VPRE phase (delay) selection

Table 110. OTP_CFG_CLOCK_1 register bit description...*continued*

Address	Register	Bit	Symbol	Value	Description
					See Table 142
		3	BOOST_CLK_SEL		BOOST clock selection
				0	BOOST_clk = CLK1 (2.22 MHz typical)
		2 to 0	BOOST_PH[2:0]		BOOST phase (delay) selection
					See Table 142

Table 111. OTP_CFG_CLOCK_2 register bit description

Address	Register	Bit	Symbol	Value	Description
0x18	OTP_CFG_ CLOCK_2	7	MOD_CONF		Clock Modulation Type Configuration
				0	Triangular modulation
				1	Pseudo random modulation
		6	MOD_EN		Clock Modulation Enable
				0	Disable
				1	Enable
		5 to 3	CLK_DIV2[2:0]		Clock 2 divider (CLK2) selection
				100	44 (CLK2 = 455 kHz typical)
		2 to 1	CLK_DIV1[1:0]		Clock 1 divider (CLK1) selection
				10	9 (CLK1 = 2.22 MHz typical)
		0	PLL_SEL		PLL enable
				0	Disabled
				1	Enabled

Table 112. OTP_CFG_FSYNC register bit description

Address	Register	Bit	Symbol	Value	Description
0x19	OTP_CFG_ FSYNC	4	FOUT_SLOT_EN		FOUT Slot release configuration
				0	FOUT not asserted high in a slot
				1	FOUT asserted high in a slot
		3 to 0	FOUTS[3:0]		FOUT sequencing assertion slot
					See Table 8 Power down slot can be changed by I2C.

Table 113. OTP_CFG_XFAILB register bit description

Address	Register	Bit	Symbol	Value	Description
0x1A	OTP_CFG_ XFAILB	6	XFAILB_PWD_CFG		XFAILB assertion impact to power down sequence

Table 113. OTP_CFG_XFAILB register bit description...*continued*

Address	Register	Bit	Symbol	Value	Description
				0	No power down when XFAILB is asserted low
				1	Power down when XFAILB is asserted low
		5 to 4	XFAILB_CFG[1:0]		Synchronization with other devices
				00	Disabled
				01	XFAILB released in a Slot (XFAILBS[3:0])
				10	XFAILB released before VPRE enable
		3 to 0	XFAILBS[3:0]		XFAILB sequencing release/assertion slot
					See Table 8 Power down slot can be changed by I2C.

Table 114. OTP_CFG_PWRUP register bit description

Address	Register	Bit	Symbol	Value	Description
0x1B	OTP_CFG_ PWRUP	7 to 4	PWRUP_LASTS[3:0]		Power up last slot assignment
				0000	Power up ends in slot 0
				0001	Power up ends in slot 1
				----	Power up ends in slot x
				1110	Power up ends in slot 14
		3 to 0	PWRDWN_FIRSTS[3:0]		Power down first slot assignment
				0000	Power down starts in slot 0
				0001	Power down starts in slot 1
				----	Power down starts in slot x
				1110	Power down starts in slot 14
				1111	Power down starts in slot 15

Table 115. OTP_CFG_TSD register bit description

Address	Register	Bit	Symbol	Value	Description
0x1C	OTP_CFG_ TSD	3	CONF_TSD_BOOST		BOOST behavior in case of TSD
				0	BOOST shutdown
				1	BOOST shutdown + go to DEEP-FS
		2	CONF_TSD_BUCK		BUCK behavior in case of TSD
				0	BUCK shutdown
				1	BUCK Shutdown + go to DEEP-FS
		1	CONF_TSD_LDO1		LDO1 behavior in case of TSD
				0	LDO1 shutdown
				1	LDO1 shutdown + go to DEEP-FS

Table 115. OTP_CFG_TSD register bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
		0	CONF_TSD_LDO2		LDO2 behavior in case of TSD
				0	LDO2 shutdown
				1	LDO2 shutdown + go to DEEP-FS

Table 116. OTP_CFG_SYS register bit description

Address	Register	Bit	Symbol	Value	Description
0x1D	OTP_CFG_ SYS	7	PWRDWN_DFS	0	When requested by fail-safe domain, go to Deep Failsafe:
				1	With power down sequence
				0	Without power down sequence
		6	LDO1_SW_EN		LDO1 Load Switch mode enable
				0	Disabled
				1	Enabled
		5	TBAT_SW_CFG		Battery short timer selection
				0	1 ms
				1	100 ms
		4	BAT_SW_EN		Battery short-circuit protection function enable
				0	Disabled
				1	Enabled
		3	VSUP_CFG		VSUP undervoltage threshold configuration
				0	4.9 V
				1	6.2 V
		2	VPRE_OFF_DLY		Delay to turn OFF VPRE at device power down
				0	250 µs
				1	32 ms
		1	AUTORETRY_INFINITE		DEEP-FS state infinite autoretry enable
				0	15 times
				1	Endless
		0	AUTORETRY_EN		DEEP-FS state autoretry enable
				0	Disabled
				1	Enabled

Table 117. OTP_CFG_VMON register bit description

Address	Register	Bit	Symbol	Value	Description
0x1E	OTP_CFG_VMON	5 to 3	VMON1_REG_ASSIGN[2:0]		Regulator assigned to VMON1
					See Table 169
		2 to 0	VMON0_REG_ASSIGN[2:0]		Regulator assigned to VMON0
					See Table 169

Table 118. OTP_CFG_I2C register bit description

Address	Register	Bit	Symbol	Value	Description
0x1F	OTP_CFG_I2C	6 to 4	VMON4_REG_ASSIGN[2:0]		Regulator assigned to VMON4
					See Table 169
		3 to 0	I2CDEVADDR[3:0]		Device Main I2C address
				0000	Address 0x20
				0001	Address 0x22
				0010	Address 0x24
				0011	Address 0x26
				0100	Address 0x28
				0101	Address 0x2A
				0110	Address 0x2C
				0111	Address 0x2E
				1000	Address 0x30
				1001	Address 0x32
				1010	Address 0x34
				1011	Address 0x36
				1100	Address 0x38
				1101	Address 0x3A
				1110	Address 0x3C
				1111	Address 0x3E

Table 119. OTP_CFG_DEVID register bit description

Address	Register	Bit	Symbol	Value	Description
0x20	OTP_CFG_DEVID	7 to 0	DeviceID[7:0]		Device ID
					Any value between 0x00 and 0xFF

19.3 Fail-safe OTP Overview

Table 120. Fail-safe OTP_REGISTERS

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OTP_CFG_VMON1	0x14	VMON1_V[7:0]							

Table 120. Fail-safe OTP_REGISTERS*...continued*

Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OTP_CFG_VMON1_ UVOV	0x15	VMON1_UVTH[3:0]				VMON1_OVTH[3:0]			
OTP_CFG_VMON2	0x16	VMON2_V[7:0]							
OTP_CFG_VMON2_ UVOV	0x17	VMON2_UVTH[3:0]				VMON2_OVTH[3:0]			
OTP_CFG_VMON3	0x18	VMON3_V[7:0]							
OTP_CFG_VMON3_ UVOV	0x19	VMON3_UVTH[3:0]				VMON3_OVTH[3:0]			
OTP_CFG_VMON_ DACx_SVS	0x1A	0	VMON4_ RINT_V	VMON0_ I2C_V	VMON123_SVS_CLAMP[4:0]				
OTP_CFG_VMON0_ UVOV	0x1B	VMON0_UVTH[3:0]				VMON0_OVTH[3:0]			
OTP_CFG_VMON4_ UVOV	0x1C	VMON4_UVTH[3:0]				VMON4_OVTH[3:0]			
OTP_CFG_VMON5_ UVOV	0x1D	VMON5_UVTH[3:0]				VMON5_OVTH[3:0]			
OTP_CFG_VMON6_ UVOV	0x1E	VMON6_UVTH[3:0]				VMON6_OVTH[3:0]			
OTP_CFG_VMON7_ UVOV	0x1F	VMON7_UVTH[3:0]				VMON7_OVTH[3:0]			
OTP_CFG_VMON8_ UVOV	0x20	VMON8_UVTH[3:0]				VMON8_OVTH[3:0]			
OTP_CFG_VMON9_ UVOV	0x21	VMON9_UVTH[3:0]				VMON9_OVTH[3:0]			
OTP_CFG_VMON_ DAC_EN_PGOOD	0x22	VMON3_ PGOOD	VMON3_ EN	VMON2_ PGOOD	VMON2_ EN	VMON1_ PGOOD	VMON1_ EN	VMON0_ PGOOD	VMON0_EN
OTP_CFG_VMON_ RES_EN	0x23	VMON7_ PGOOD	VMON7_ EN	VMON6_ PGOOD	VMON6_ EN	VMON5_ PGOOD	VMON5_ EN	VMON4_ PGOOD	VMON4_EN
OTP_CFG_VMON_ RES_PGOOD	0x24	0	0	0	0	VMON9_ PGOOD	VMON9_ EN	VMON8_ PGOOD	VMON8_EN
OTP_CFG_ABIST1_ VMON_DAC_RSTB	0x25	ABIST1_ VMON7	ABIST1_ VMON6	ABIST1_ VMON5	ABIST1_ VMON4	ABIST1_ VMON3	ABIST1_ VMON2	ABIST1_ VMON1	ABIST1_ VMON0
OTP_CFG_ABIST1_ VMON_RES	0x26	0	0	0	RSTB_[1] 8S_DIS	RSTB_DLY	RSTB2 PGOOD	ABIST1_ VMON9	ABIST1_ VMON8
OTP_CFG_WD_ FCCU	0x27	0	0	0	WD_DIS	WD_ SELECTION	ERRMON_ EN	FCCU_EN	FLT_ RECOVERY _EN
OTP_CFG_DGLT_ VMON12	0x28	VMON1_UV_ DGLT[1:0]		VMON1_OV_ DGLT[1:0]		VMON04_UV_DGLT[1:0]		VMON04_OV_DGLT[1:0]	
OTP_CFG_DGLT_ VMON3	0x29	VMON3_UV_ DGLT[1:0]		VMON3_OV_ DGLT[1:0]		VMON2_UV_DGLT[1:0]		VMON2_OV_DGLT[1:0]	
OTP_CFG_DGLT_ VMON_RES	0x2A	VMON789_ UV_DGLT[1:0]		VMON789_ OV_DGLT[1:0]		VMON56_UV_DGLT[1:0]		VMON56_OV_DGLT[1:0]	
OTP_CFG_I2C	0x2B	0	0	0		I2CDEVID[3:0]			

[1] Can be changed later by I2C

19.4 Fail-safe OTP bit description

Table 121. Fail-safe OTP bit description

Address	Register	Bit	Symbol	Value	Description
0x14	OTP_CFG_VMON1	7 to 0	VMON1_V[7:0]		VMON1 monitoring voltage
					See Table 161
0x15	OTP_CFG_VMON1_UVOV	7 to 4	VMON1_UVTH[3:0]		VMON1 undervoltage threshold
					See Table 163
		3 to 0	VMON1_OVTH[3:0]		VMON1 overvoltage threshold
					See Table 163
0x16	OTP_CFG_VMON2	7 to 0	VMON2_V[7:0]		VMON2 monitoring voltage
					See Table 161
0x17	OTP_CFG_VMON2_UVOV	7 to 4	VMON2_UVTH[3:0]		VMON2 undervoltage threshold
					See Table 163
		3 to 0	VMON2_OVTH[3:0]		VMON2 overvoltage threshold
					See Table 163
0x18	OTP_CFG_VMON3	7 to 0	VMON3_V[7:0]		VMON3 monitoring voltage
					See Table 161
0x19	OTP_CFG_VMON3_UVOV	7 to 4	VMON3_UVTH[3:0]		VMON3 undervoltage threshold
					See Table 163
		3 to 0	VMON3_OVTH[3:0]		VMON3 overvoltage threshold
					See Table 163
0x1A	OTP_CFG_VMON_DACx_SVS	6	VMON4_RINT_V		VMON4 monitoring voltage
				0	1.8V
				1	3.3V
		5	VMON0_I2C_V		VMON0 monitoring voltage
				0	1.8V
				1	3.3V
		4 to 0	VMON123_SVS_CLAMP[4:0]		SVS max value allowed (mask)
				00000	No SVS
				00001	2 steps allowed (0 to -6.25 mV)
				00011	4 steps allowed (0 to -18.75 mV)
				00111	8 steps allowed (0 to -43.75 mV)
				01111	16 steps allowed (0 to -93.75 mV)
				11111	32 steps allowed (0 to -193.75 mV)
0x1B	OTP_CFG_VMON0_UVOV	7 to 4	VMON0_UVTH[3:0]		VMON0 undervoltage threshold
					See Table 163
		3 to 0	VMON0_OVTH[3:0]		VMON0 overvoltage threshold

Table 121. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
					See Table 163
0x1C	OTP_CFG_VMON4_UVOV	7 to 4	VMON4_UVTH[3:0]		VMON4 undervoltage threshold
					See Table 163
		3 to 0	VMON4_OVTH[3:0]		VMON4 overvoltage threshold
					See Table 163
0x1D	OTP_CFG_VMON5_UVOV	7 to 4	VMON5_UVTH[3:0]		VMON5 undervoltage threshold
					See Table 163
		3 to 0	VMON5_OVTH[3:0]		VMON5 overvoltage threshold
					See Table 163
0x1E	OTP_CFG_VMON6_UVOV	7 to 4	VMON6_UVTH[3:0]		VMON6 undervoltage threshold
					See Table 163
		3 to 0	VMON6_OVTH[3:0]		VMON6 overvoltage threshold
					See Table 163
0x1F	OTP_CFG_VMON7_UVOV	7 to 4	VMON7_UVTH[3:0]		VMON7 undervoltage threshold
					See Table 163
		3 to 0	VMON7_OVTH[3:0]		VMON7 overvoltage threshold
					See Table 163
0x20	OTP_CFG_VMON8_UVOV	7 to 4	VMON8_UVTH[3:0]		VMON8 undervoltage threshold
					See Table 163
		3 to 0	VMON8_OVTH[3:0]		VMON8 overvoltage threshold
					See Table 163
0x21	OTP_CFG_VMON9_UVOV	7 to 4	VMON9_UVTH[3:0]		VMON9 undervoltage threshold
					See Table 163
		3 to 0	VMON9_OVTH[3:0]		VMON9 overvoltage threshold
					See Table 163
0x22	OTP_CFG_VMON_DAC_EN_PGOOD	7	VMON3_PGOOD		VMON3 assignment to PGOOD
				0	Not assigned
				1	Assigned
		6	VMON3_EN		VMON3 monitoring enable
				0	Disabled
				1	Enabled
		5	VMON2_PGOOD		VMON2 assignment to PGOOD
				0	Not assigned
				1	Assigned
		4	VMON2_EN		VMON2 monitoring enable
				0	Disabled

Table 121. Fail-safe OTP bit description *...continued*

Address	Register	Bit	Symbol	Value	Description
				1	Enabled
		3	VMON1_PGOOD		VMON1 assignment to PGOOD
				0	Not assigned
				1	Assigned
		2	VMON1_EN		VMON1 monitoring enable
				0	Disabled
				1	Enabled
		1	VMON0_PGOOD		VMON0 assignment to PGOOD
				0	Not assigned
				1	Assigned
		0	VMON0_EN		VMON0 monitoring enable
				0	Disabled
				1	Enabled
0x22	OTP_CFG_VMON_DAC_ EN_PGOOD	7	VMON7_PGOOD		VMON7 assignment to PGOOD
				0	Not assigned
				1	Assigned
		6	VMON7_EN		VMON7 monitoring enable
				0	Disabled
				1	Enabled
		5	VMON6_PGOOD		VMON6 assignment to PGOOD
				0	Not assigned
				1	Assigned
		4	VMON6_EN		VMON6 monitoring enable
				0	Disabled
				1	Enabled
		3	VMON5_PGOOD		VMON5 assignment to PGOOD
				0	Not assigned
				1	Assigned
		2	VMON5_EN		VMON5 monitoring enable
				0	Disabled
				1	Enabled
		1	VMON4_PGOOD		VMON4 assignment to PGOOD
				0	Not assigned
				1	Assigned
		0	VMON4_EN		VMON4 monitoring enable
				0	Disabled

Table 121. Fail-safe OTP bit description...*continued*

Address	Register	Bit	Symbol	Value	Description
				1	Enabled
0x24	OTP_CFG_VMON_RES_PGOOD	3	VMON9_PGOOD		VMON9 assignment to PGOOD
				0	Not assigned
				1	Assigned
		2	VMON9_EN		VMON9 monitoring enable
				0	Disabled
				1	Enabled
		1	VMON8_PGOOD		VMON8 assignment to PGOOD
				0	Not assigned
				1	Assigned
		0	VMON8_EN		VMON8 monitoring enable
				0	Disabled
				1	Enabled
0x25	OTP_CFG_ABIST1_VMON_DAC_RSTB	7	ABIST1_VMON7		VMON7 assignment to ABIST1
				0	Not assigned
				1	Assigned
		6	ABIST1_VMON6		VMON6 assignment to ABIST1
				0	Not assigned
				1	Assigned
		5	ABIST1_VMON5		VMON5 assignment to ABIST1
				0	Not assigned
				1	Assigned
		4	ABIST1_VMON4		VMON4 assignment to ABIST1
				0	Not assigned
				1	Assigned
		3	ABIST1_VMON3		VMON3 assignment to ABIST1
				0	Not assigned
				1	Assigned
		2	ABIST1_VMON2		VMON2 assignment to ABIST1
				0	Not assigned
				1	Assigned
		1	ABIST1_VMON1		VMON1 assignment to ABIST1
				0	Not assigned
				1	Assigned
		0	ABIST1_VMON0		VMON0 assignment to ABIST1
				0	Not assigned

Table 121. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
				1	Assigned
0x26	OTP_CFG_ABIST1_VMON_RES	4	RSTB_8S_DIS		Device goes DEEP-FS if RSTB stays low level longer than 8 seconds
				0	Activated
				1	Deactivated
		3	RSTB_DLY		Delay after ABIST1 is done and before RSTB pin is released
				0	No Delay
				1	10ms delay
		2	PGOOD2RSTB		RSTB assignment to PGOOD
				0	Not assigned
				1	Assigned
		1	ABIST1_VMON9		VMON9 assignment to ABIST1
				0	Not assigned
				1	Assigned
		0	ABIST1_VMON8		VMON8 assignment to ABIST1
				0	Not assigned
				1	Assigned
0x27	OTP_CFG_WD_FCCU	4	WD_DIS		Watchdog monitoring enable
				0	Enabled
				1	Disabled
		3	WD_SELECTION		Watchdog mode selection
				0	Simple WD
				1	Challenger WD
		2	ERRMON_EN		ERRMON monitoring enable
				0	Disabled
				1	Enabled
		1	FCCU_EN		FCCU monitoring enable
				0	Disabled
				1	Enabled
		0	FLT_RECOVERY_EN		Fault recovery strategy enable
				0	Disabled
				1	Enabled
0x28	OTP_CFG_DGLT_VMON12	7 to 6	VMON1_UV_DGLT[1:0]		VMON1 undervoltage filtering time
					See Table 165
		5 to 4	VMON1_OV_DGLT[1:0]		VMON1 overvoltage filtering time

Table 121. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
					See Table 165
		3 to 2	VMON04_UV_DGLT[1:0]		VMON0 and VMON4 undervoltage filtering time
					See Table 165
		1 to 0	VMON04_OV_DGLT[1:0]		VMON0 and VMON4 overvoltage filtering time
					See Table 165
0x29	OTP_CFG_DGLT_VMON3	7 to 6	VMON3_UV_DGLT[1:0]		VMON3 undervoltage filtering time
					See Table 165
		5 to 4	VMON3_OV_DGLT[1:0]		VMON3 overvoltage filtering time
					See Table 165
		3 to 2	VMON2_UV_DGLT[1:0]		VMON2 undervoltage filtering time
					See Table 165
		1 to 0	VMON2_OV_DGLT[1:0]		VMON2 overvoltage filtering time
					See Table 165
0x2A	OTP_CFG_DGLT_VMON_RES	7 to 6	VMON789_UV_DGLT[1:0]		VMON7, VMON8, VMON9 undervoltage filtering time
					See Table 165
		5 to 4	VMON789_OV_DGLT[1:0]		VMON7, VMON8, VMON9 overvoltage filtering time
					See Table 165
		3 to 2	VMON56_UV_DGLT[1:0]		VMON5, VMON6 undervoltage filtering time
					See Table 165
		1 to 0	VMON56_OV_DGLT[1:0]		VMON5, VMON6 overvoltage filtering time
					See Table 165
0x2B	OTP_CFG_I2C	3 to 0	I2CDEVID[3:0]		Device fail-safe I2C address
				0000	Address 0x21
				0001	Address 0x23
				0010	Address 0x25
				0011	Address 0x27
				0100	Address 0x29
				0101	Address 0x2B
				0110	Address 0x2D
				0111	Address 0x2F
				1000	Address 0x31
				1001	Address 0x33

Table 121. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
				1010	Address 0x35
				1011	Address 0x37
				1100	Address 0x39
				1101	Address 0x3B
				1110	Address 0x3D
				1111	Address 0x3F

20 BOS: Best Of Supply

20.1 Functional description

BOS regulator manages the best of supply from VSUP and VBOOST pins to efficiently generate 5.0 V output to supply the internal biasing of the device. VBOS is also the supply of VPRE high-side and low-side gate drivers and VBOOST low-side gate driver.

VBOS undervoltage may not guarantee the full functionality of the device. Consequently, $V_{BOS} < V_{BOS\_UVL}$ detection powers down the device.

V_{SUP_UV7} undervoltage threshold is used to enable the path from VSUP to VBOS when $V_{SUP} < V_{SUP\_UV7}$ to have a low drop path from VSUP, while VPRE is going low and to power up the device when VPRE is not started. When $V_{SUP} > V_{SUP\_UV7}$, VBOS is forced to use VBOOST to optimize the efficiency.

20.2 BOS electrical characteristics

Table 122. Best of supply electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Best of supply					
V_{BOS}	Best of supply output voltage at VBOS pin	3.3	5.0	5.25	V
V_{BOS_UVH}	V_{BOS} undervoltage threshold high (V_{BOS} rising)	4.1	4.3	4.5	V
V_{BOS_UVL}	V_{BOS} undervoltage threshold low (V_{BOS} falling)	3.2	3.3	3.4	V
T_{BOS_UV}	V_{BOS_UVH} and V_{BOS_UVL} filtering time	6.0	10	15	µs
V_{BOS_POR}	V_{BOS} power on reset threshold	—	—	2.5	V
T_{BOS_POR}	V_{BOS_POR} filtering time	0.5	—	1.5	µs
I_{BOS}	Best of supply current capability	—	—	60	mA
$V_{dropout\_VBOOST}$	Maximum dropout voltage (I_{BOS} = 60mA)			250	mV
C_{OUT_BOS}	Effective output capacitor	3.0	4.7	13	µF
	Output decoupling capacitor	—	0.1	—	µF

21 Power Management

Table 123. Power management

Regulator	Type	Input Supply	Output Range	Max DC current
VPRE	HV Buck controller	4.5 V to 60 V	3.3 V to 5.0 V	15 A
BOOST	Boost regulator	VPRE	5.0 V to 6.0 V	1.0 A
BUCK	Buck regulator	VPRE	1.0 V to 3.3 V	2.5 A
LDO1	Linear regulator with load switch capability	VPRE, BUCK or BOOST	1.5 V to 5.0 V	400 mA
LDO2	Linear regulator	BOOST	1.1 V to 5.0 V	400 mA

The FS86 starts when $V_{SUP} > V_{SUP\_UVH}$, with VBOS first, followed by VPRE, and the power up sequencing from the OTP programming for the remaining regulators (BOOST, BUCK, LDO1, LDO2).

22 VPRE: High voltage buck regulator

22.1 Functional description

VPRE block is a high voltage, synchronous, peak current mode buck controller. VPRE works with external N-type MOSFETs in forced PWM Continuous Conduction Mode (CCM) at 455 kHz or 2.22 MHz. VPRE input voltage is naturally limited to $V_{SUP} = L_{PRE\_DCR} \times I_{PRE} + V_{PRE\_UVL} / D_{MAX}$ with $D_{MAX} = 1 - (F_{PRE\_SW} \times T_{PRE\_OFF\_MIN})$.

A bootstrap capacitor is required to supply the gate drive circuit of the high-side MOS. The output voltage is configurable by OTP from 3.3 V to 5.0 V, and the switching frequency is configurable by OTP at 455 kHz for 12 V and 24 V transportation applications or 2.22 MHz for 12 V automotive applications. The stability is ensured by an external Type 2 compensation network with slope compensation.

The maximum current capability is defined by the external components (MOS gate charge, inductor, shunt resistor), the gate driver current capability and the switching frequency. An overcurrent detection is implemented to protect the external MOSFETs.

The output current is sensed externally via inductor lossless DCR sensing technique or a shunt resistor in series with the inductor. An over-current protection is available to limit the maximum sensed voltage and can be configured by OTP VPREILIM[1:0] bits between 50 mV and 150 mV.

If an overcurrent is detected after the HS minimum ON-time, the HS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on VPRE and/or one of the cascaded regulators.

The maximum input voltage is 60 V and allows operation in 24 V truck applications without external protection to sustain ISO 16750-2:2012 load dump pulse 5b. VPRE must be the input supply of the BOOST and BUCK. VPRE can be the input supply of LDO1. VPRE can be the supply of local loads remaining inside the ECU.

By default, VPRE switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied at FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

V_{PRE_UVH}, V_{PRE_UVL} and $V_{PRE\_FB\_OV}$ thresholds are monitored from PRE_FB pin and manage some transitions of the main state machine described in Section 14.1 "Simplified functional state diagram". These types of monitoring are not safety related.

22.2 Application schematic with Rshunt current sensing

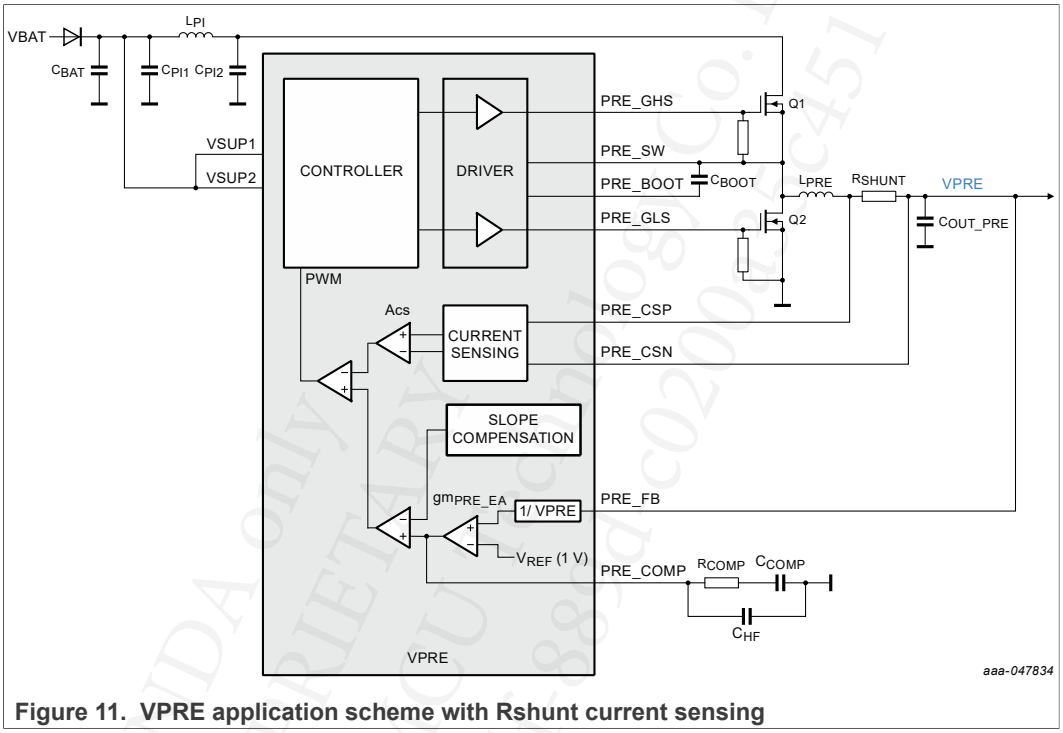


Figure 11. VPRE application scheme with Rshunt current sensing

22.3 Application schematic with lossless DCR current sensing

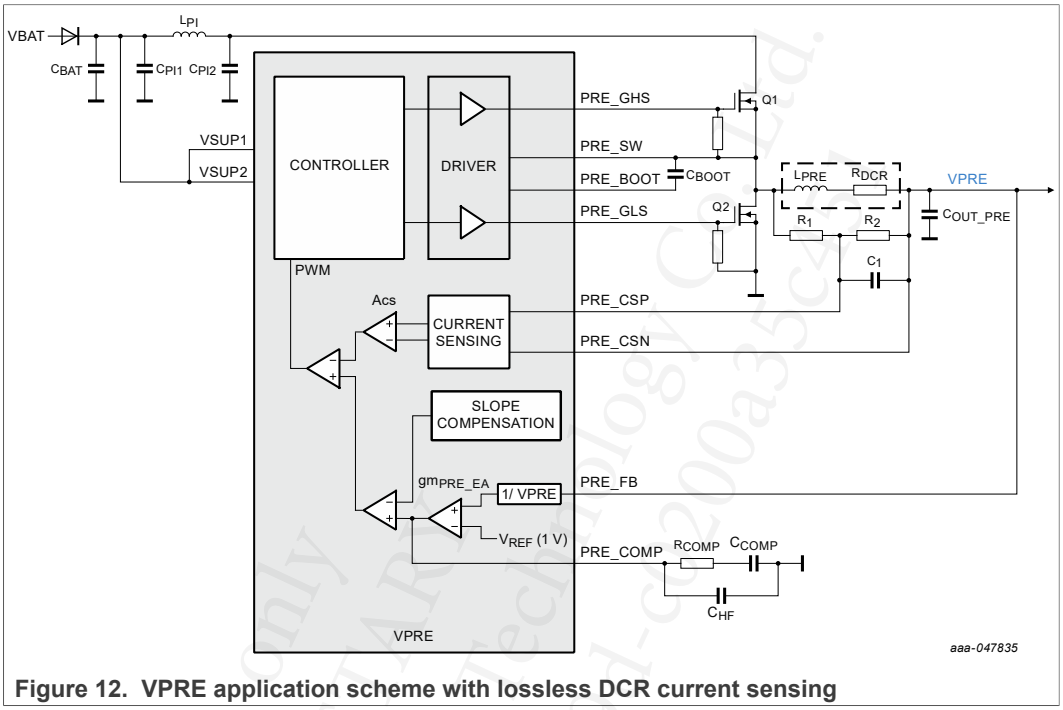


Figure 12. VPRE application scheme with lossless DCR current sensing

22.4 Current sensing

22.4.1 Shunt sense

The current sense can be done using a shunt resistor R_{SHUNT} in series with the VPRE inductor L_{PRE}, as shown in Figure 11. VPRE application schematic with Rshunt current sensing.

22.4.2 Lossless DCR sense

For high current applications (I_{PRE} > 5 A), the power dissipation in the current sense resistor becomes non-negligible (> 0.25 W). In that case, the DCR current sense technique can be a good alternative, using the intrinsic DCR of the inductor to sense the current, as shown in Figure 12. However, the inductor DCR value is less accurate than a shunt resistor which impacts the current limitation. Higher resistance value means lower current limitation and less accuracy means wider current limitation range.

22.4.2.1 Low DCR value

When the inductor DCR is low (lower than 15 mΩ as a guideline only), the DCR current sense with a single capacitor C1 is possible. In this case, the current limitation is linked to the inductor DCR value ($I_{LIM\_PRE} = V_{PRE\_LIM\_TH}$ / DCR). When R1 and C1 are selected in such a way that the RC time constant is equal to the ratio of inductance and its series resistance, the voltage across C1 is directly proportional to the inductor current.

$R1 \times C1 = L_{PRE}$ / DCR

To select R1 and C1, start by taking capacitor C1 in the range of hundred nF to obtain a resistor R1 in the kΩ range, then calculate the other component. Example for an inductor L = 6.8 µH and DCR = 10 mΩ:

- C1 = 100 nF, then R1 = 6.8 kΩ
- I_{LIM_PRE} = 12 A for $V_{PRE\_LIM\_TH}$ = 120 mV

22.4.2.2 High DCR value

When the inductor DCR is high (higher than 15 mΩ as a guideline only), the DCR current sense with a resistor divider (R1 + R2) helps to maintain a high current limitation by feeding a ratio of the current to the differential amplifier. In that case, the current limitation is linked to the voltage across the R2 resistor. When R1 and C1 are selected in such a way that the RC time constant is equal to the ratio of inductance and its series resistance, the voltage across C1 is directly proportional to the inductor current.

(R1 // R2) × C1 = L_{VPRE} / DCR

To select R1 and C1, start by taking capacitor C1 in the range of hundred nF to obtain resistors R1 and R2 in the kΩ range, then calculate the other components. Example for an inductor L = 6.8 µH and DCR = 20 mΩ:

- I_{LIM_PRE} = 12 A for $V_{PRE\_LIM\_TH}$ = 120 mV;
- C1 is selected at 100 nF;
- R1 and R2 are calculated.

Table 124. High DCR values

Parameter	Value	Unit	Comments
L_{PRE}	6.8	uH	
RDR	20	mΩ	
$V_{PRE\_LIM\_TH}$	120	mV	VPREILIM (OTP)
Ipre_max	12	A	
R_{SENSE}	10	mΩ	$V_{PRE\_LIM\_TH}$ / I_{LIM_PRE}
Ratio	2.0		DCR / R_{SENSE}
C1	100	nF	Selected
R1	6.80	kΩ	L_{PRE} / (R_{SENSE} x C1)
R2	6.80	kΩ	R1 / (Ratio - 1)
V_Lpre	240	mV	DCR x I_{LIM_PRE}
VR2	120	mV	V_Lpre x R2 / (R2 + R1)

22.5 External components

A PI filter, with cutoff frequency $f_C = 1 / [2\pi \times \sqrt{(L_{PI}\ C_{PI1})}] < f_{PRE\_SW} / 10$, is required to filter VPRE switching frequency F_{PRE_SW} on the battery line. VSUP1,2 two pins must be connected on the battery side of the PI filter for a clean biasing of the device. C_{PI1} capacitor must be implemented close to VSUP1,2 pins. C_{PI2} capacitor must be implemented close to VPRE high-side MOSFET Q1.

The bootstrap capacitor value should be sized to be at least 15 times larger than the HS gate charge ($Q_{G(tot)}$) divided by V_{PRE_DRV}.

It is recommended to place gate to source resistors on Q1 and Q2 to guarantee a passive switch OFF of the transistors in case of pin disconnection.

22.6 Compensation network and stability

The external compensation network, made with R_{COMP}, C_{COMP} and C_{HF} must be calculated for best compromise between stability and transient response, based on below conceptual plot of Type 2 compensation network transfer function.

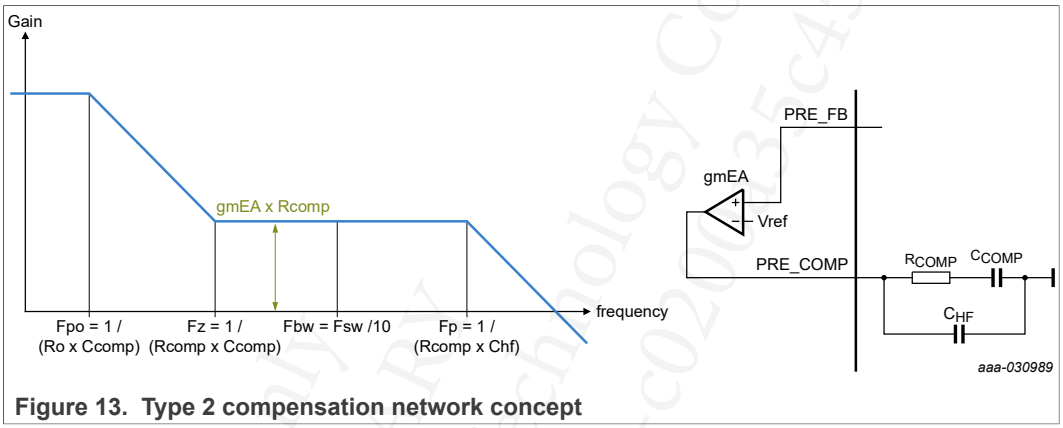


Figure 13. Type 2 compensation network concept

Calculation guideline:

- System bandwidth for F_{PRE_SW} = 455 kHz: $F_{bw} = F_{PRE\_SW} / 10$ = 45 kHz
- System bandwidth for F_{PRE_SW} = 2.22 MHz: $F_{bw} = F_{PRE\_SW} / 18$ = 123 kHz
- Compensation zero: $Fz = F_{bw} / 10$
- Compensation pole: $F_p = F_{PRE\_SW} / 2$
- $R_{SENSE} = R_{SHUNT}$ or DCR equivalent value
- Open-loop cutoff frequency: $F_{GBW} = 1 / (2\pi \times R_{SENSE} \times A_{CS} \times C_{OUT\_PRE})$
- Error amplifier gain: $EA\_gain = (V_{REF} / V_{PRE}) \times gm_{PRE\_EA} \times R_{COMP} = 10 \text{ ^ } LOG (F_{BW} / F_{GBW})$
- V_{REF} = 1.0 V
- $R_{COMP} = V_{PRE} \times (EA\_gain / gm_{PRE\_EA})$
- $C_{COMP} = 1 / (2\pi \times Fz \times R_{COMP})$
- $C_{HF} = 1 / (2\pi \times Fp \times R_{COMP})$
- Slope compensation: $Se \geq (V_{PRE} / L_{VPRE}) \times R_{SENSE} \times A_{CS}$

The compensation network can be automatically calculated with the FS86 GUI that uses the same formulas. A Simplis simulation is recommended to verify the Phase and Gain Margin with normalized components.

Use case calculation with V_{PRE} = 4.1 V, L_{VPRE} = 6.8 µH, F_{PRE_SW} = 455 kHz, C_{OUT_PRE} = 66 µF, R_{SHUNT} = 10.0 mΩ:

- System bandwidth: F_{bw} = 45 kHz
- Compensation zero: Fz = 4.5 kHz
- Compensation pole: Fp = 227 kHz
- F_{GBW} = 53 kHz
- Error amplifier gain: $EA\_gain = 10 \text{ ^ } LOG (F_{BW} / F_{GBW})$ = 0.86
- R_{COMP} = 2.34 kΩ → 2.2 kΩ
- C_{COMP} = 15.9 nF → 16 nF

- C_{HF} = 318 pF → 330 pF
- Slope compensation: Se > 30 mV/µs

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

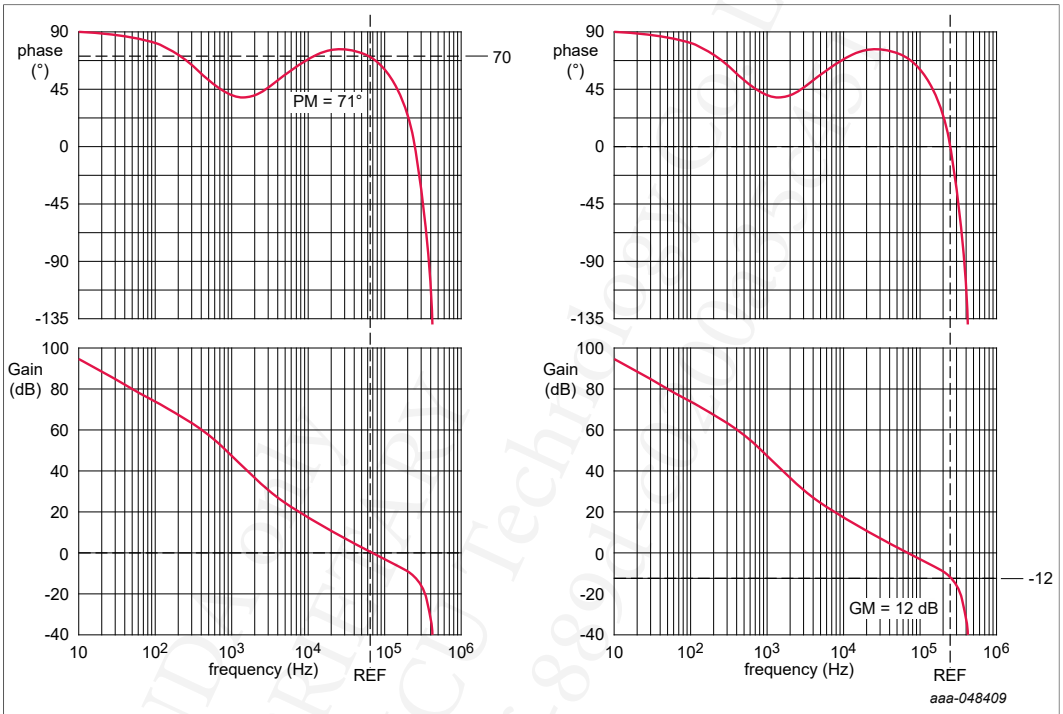


Figure 14. VPRE phase and margin simulation

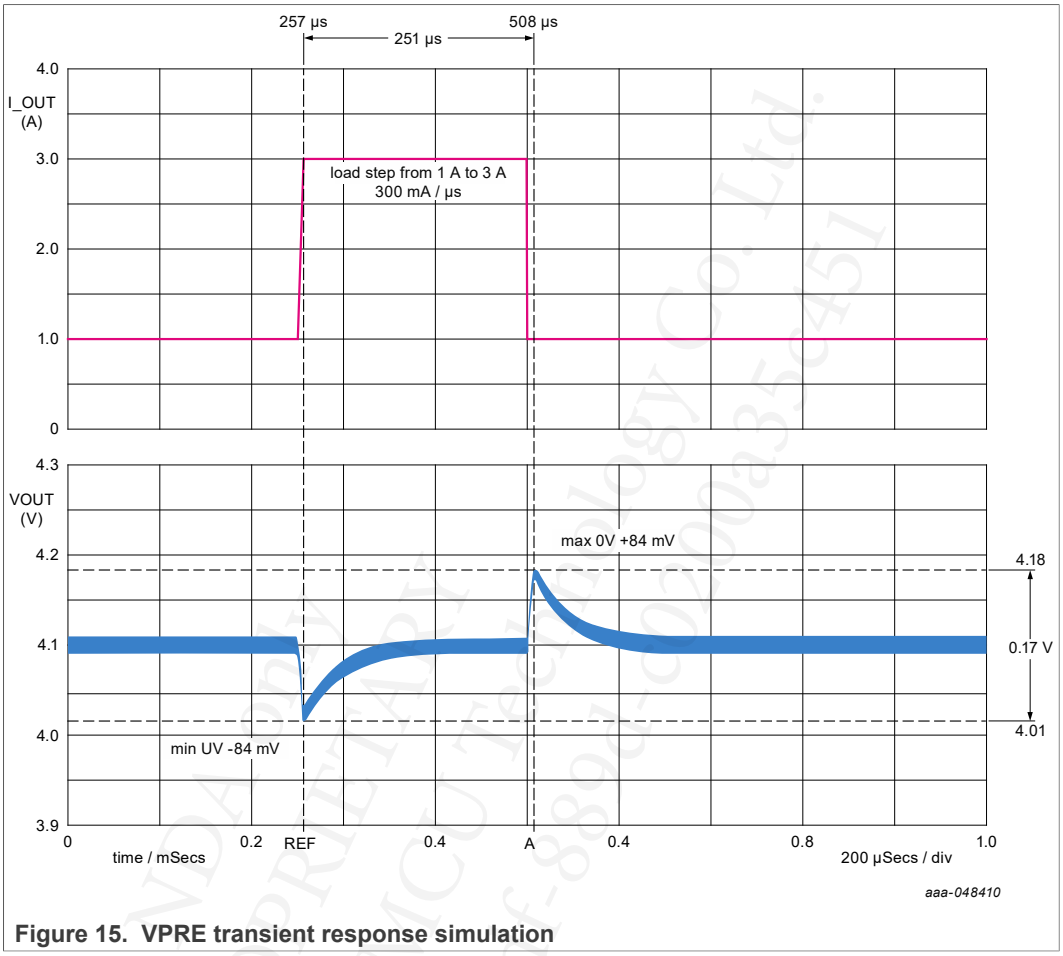


Figure 15. VPRE transient response simulation

22.7 Electrical characteristics

Table 125. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Static Electrical Characteristics					
V_{PRE}	Output Voltage (OTP VPREV[5:0] configurable)	3.3	—	5.0	V
	Configuration step	—	0.1	—	V
	Accuracy	−3.0	—	3.0	%
$T_{PRE\_SOFT\_START}$	Output voltage from 10 % to 90 % OTP VPRESSRAMP = 0 OTP VPRESSRAMP = 1	 500 250	 900 450	 1300 650	 µs
	Digital DAC soft start completion	—	—	1.35	ms
F_{PRE_SW}	Switching Frequency Range OTP VPRE_CLK_SEL = 0 OTP VPRE_CLK_SEL = 1	 2.10 430	 2.22 455	 2.35 480	 MHz kHz

Table 125. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
I_{PRE}	DC output current capability				
	OTP VPRE_CLK_SEL = 0 (2.22 MHz)	—	—	6	A
	OTP VPRE_CLK_SEL = 1 (455 kHz)	—	—	15	
$V_{PRE\_FB\_OV}$	Ratio-metric overvoltage threshold protection	1.15x VPRE	—	1.23x VPRE	V
$T_{PRE\_FB\_OV}$	$V_{PRE\_FB\_OV}$ filtering time	1.0	2.0	3.0	µs
V_{PRE_UVH}	Under voltage threshold high	2.9	—	3.1	V
V_{PRE_UVL}	Under voltage threshold low	2.5	—	2.7	V
T_{PRE_UV}	V_{PRE_UVH} and V_{PRE_UVL} filtering time	6.0	10	15	µs
$T_{VPRE\_UV\_DFS}$	Start-up time-out to reach V_{PRE} > V_{PRE_UVL}	3.6	4.0	4.4	ms
$T_{VPRE\_OFF\_DLY}$	Delay between slot 0 and VPRE turn-off				
	OTP VPRE_OFF_DLY = 0	—	250	—	µs
	OTP VPRE_OFF_DLY = 1	—	32	—	ms
gm_{PRE_EA}	Error amplifier transconductance	1.28	1.50	1.84	mS
A_{CS}	Current sense amplifier gain	4.5	5.0	5.5	V/V
V_{PRE_SLOPE}	Slope compensation				mV/µs
	OTP VPRESC[5:0] = 000010	15.7	20.7	26.0	
	OTP VPRESC[5:0] = 000011	23.6	31.1	39.0	
	OTP VPRESC[5:0] = 000100	31.3	41.4	52.0	
	OTP VPRESC[5:0] = 000101	39.1	51.8	65.0	
	OTP VPRESC[5:0] = 000110	47.1	62.1	77.9	
	OTP VPRESC[5:0] = 000111	54.9	72.5	90.9	
	OTP VPRESC[5:0] = 001000	61.1	82.5	105	
	OTP VPRESC[5:0] = 001001	69.0	92.8	118	
	OTP VPRESC[5:0] = 001010	77.1	103	131	
	OTP VPRESC[5:0] = 001011	85.0	114	143	
	OTP VPRESC[5:0] = 001100	92.8	124	156	
	OTP VPRESC[5:0] = 001101	100	134	169	
	OTP VPRESC[5:0] = 001110	109	145	182	
	OTP VPRESC[5:0] = 001111	117	155	195	
	OTP VPRESC[5:0] = 010000	131	175	221	
	OTP VPRESC[5:0] = 010001	147	196	247	
	OTP VPRESC[5:0] = 010010	163	217	273	
	OTP VPRESC[5:0] = 010011	179	237	299	
	OTP VPRESC[5:0] = 010100	194	258	324	
$T_{PRE\_ON\_MIN}$	HS minimum ON time				
	VPRETON[1:0] = 01	39	65	91	ns
	VPRETON[1:0] = 10	15	25	35	
$T_{PRE\_OFF\_MIN}$	HS minimum OFF time				
	VPRETOFF[1:0] = 00	40	80	120	ns

Table 125. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PRE\_LIM\_TH}$	Forward current limit (sense amplifier peak detection threshold) OTP VPREILIM[1:0] = 00 OTP VPREILIM[1:0] = 01 OTP VPREILIM[1:0] = 10 OTP VPREILIM[1:0] = 11	 35 60 96 127	 50 80 120 150	 65 100 144 180	mV
$V_{PRE\_VALLEY\_LIM\_TH}$	Reverse current limit (sense amplifier valley detection threshold)	−65	−50	−35	mV
V_{PRE_DRV}	HS and LS gate driver output voltage	—	VBOS	—	V
$I_{PRE\_GATE\_DRV}$	HS and LS gate driver pullup and pulldown current capability OTP VPRESRHS[1:0] and VPRESRLS[1:0] bits by default, VPRESRHS_RISE[1:0], VPRESRHS_FALL[1:0], VPRESRLS[1:0] bits by I2C VPRESR[1:0] = 00 VPRESR[1:0] = 01 VPRESR[1:0] = 10 VPRESR[1:0] = 11	 90 180 360 630	 130 260 520 900	 200 400 800 1400	mA
R_{DIS}	Discharge resistance when disabled	250	500	1000	Ω
$I_{PRE\_SW\_LKG}$	PRE_SW leakage	—	—	6.0	µA
R_{DRV_OFF}	HS and LS gate driver pull down resistor when VPRE is disabled	5.0	—	35	kΩ
R_{BOOT_OFF}	PRE_BOOT pull down resistor when VPRE is disabled	1.2	1.7	2.6	kΩ
I_{BOOT_LKG}	PRE_BOOT leakage	—	—	10	µA
BAT_SW protection					
T_{BAT_SW}	BAT_SW timer OTP TBAT_SW_CFG xor I2C TBAT_SW_CFG = 0 OTP TBAT_SW_CFG xor I2C TBAT_SW_CFG = 1	 0.9 90	 1.0 100	 1.1 110	ms
$V_{PRE\_SW\_OV}$	BAT_SW protection overvoltage threshold to go DEEP-FS	3.3	3.6	3.9	V
$T_{PRE\_SW\_OV}$	$V_{PRE\_SW\_OV}$ filtering time	1.0	2.0	3.0	µs
Transient Electrical Characteristics					
$V_{PRE\_LINE\_REG\_455k}$	Transient line regulation at 455 kHz V_{SUP} = 6.0 V to 18 V and V_{SUP} = 12 V to 36 V (C_{IN_PRE} = 20 uF + PI filter, L_{PRE} = 6.8 µH, C_{OUT_PRE} > 100 µF, dv/dt = 100 mV/µs)	−3.0	—	3.0	%
$V_{PRE\_LINE\_REG\_2.2M}$	Transient line regulation at 2.22 MHz V_{SUP} = 6.0 V to 18 V (C_{IN_PRE} = 20 uF + PI filter, L_{PRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, dv/dt = 100 mV/µs)	−3.0	—	3.0	%

Table 125. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PRE\_LOAD\_REG\_455k}$	Transient load regulation at 455 kHz V_{SUP} = 6.0 V to 36 V, V_{PRE} = 3.3 V (L_{PRE} = 6.8 µH, C_{OUT_PRE} > 100 µF, from 5.0 A to 10 A, di/dt = 300 mA/µs)	−3.0	—	3.0	%
$V_{PRE\_LOAD\_REG\_2.2M}$	Transient load regulation at 2.22MHz V_{SUP} = 6.0 V to 18 V, V_{PRE} = 3.3 V (L_{PRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, from 1.0 A to 3.0 A, di/dt = 300 mA/µs)	−3.0	—	3.0	%
$V_{PRE\_RIPPLE\_455k}$	VPRE voltage ripple at 455 kHz V_{SUP} = 12 V and V_{SUP} = 24 V (L_{PRE} = 6.8 µH, C_{OUT_PRE} > 100 µF, V_{PRE} = 3.3 V and 5.0 V, I_{PRE} = 5.0A)	−1.0	—	1.0	%
$V_{PRE\_RIPPLE\_2.2M}$	VPRE voltage ripple at 2.22 MHz V_{SUP} = 12 V (L_{PRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, V_{PRE} = 3.3 V and 5.0 V, I_{PRE} = 3.0A)	−0.5	—	0.5	%
I_{LIM_PRE}	Inductor peak current limitation range R_{SHUNT} = 8 mΩ and $V_{PRE\_LIM\_TH}$ = 150 mV (To be recalculated for different R_{SHUNT} and different $V_{PRE\_LIM\_TH}$) I_{LIM_PRE} = $V_{PRE\_LIM\_TH}$ / R_{SHUNT}	15.9	18.8	22.5	A
External components					
C_{IN_PRE}	Effective input capacitor (C_{PI2})	20	—	—	µF
	Input decoupling capacitor	—	0.1	—	µF
C_{OUT_PRE}	Effective output capacitor OTP VPRE_CLK_SEL = 0 (2.22 MHz) OTP VPRE_CLK_SEL = 1 (455 kHz)	 20 40	 44 100	 110 300	µF
L_{PRE}	Inductor OTP VPRE_CLK_SEL = 0 (2.22 MHz) OTP VPRE_CLK_SEL = 1 (455 kHz)	 1.5 2.2	 2.2 4.7	 4.7 10	µH
R_{SHUNT}	Current sense resistor (SHUNT)	8.0	—	20	mΩ
R_{DCR}	Inductor DCR ***Note:*** *When using DCR (loss-less) current sense, L_{PRE} (µH)* OTP VPRE_CLK_SEL = 0 (2.22 MHz) OTP VPRE_CLK_SEL = 1 (455 kHz)	 8.0x L_{PRE} 1.5x L_{PRE}	 — —	 — —	mΩ
$Q_{G(tot)}$	External MOSFET total gate charge (V_{GS} = 5.0 V) OTP VPRE_CLK_SEL = 0 (2.22 MHz) OTP VPRE_CLK_SEL = 1 (455 kHz)	 — —	 — —	 7 15	nC
$V_{GS(th)}$	External MOSFET gate-source threshold voltage **Note:** shall logic level compatible MOSFETs	—	1.8	2.5	V

Table 125. Electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DS_Max}	External MOSFET maximum drain-source voltage				
	12 V automotive applications	40	—	—	V
	24 V truck/bus applications	60	—	—	

22.8 VPRE external MOSFETs

Other MOSFETs can be used, but should have performances similar to the recommended references.

Table 126. Recommended references

Application	F_{PRE_SW}	I_{PRE} < 6.0 A	I_{PRE} < 10 A	I_{PRE} > 10 A
12 V	455 kHz	BUK9K18-40E	BUK9K12-60E	HS: BUK9M9R5-40H LS: BUK9M3R3-40H
	2.22 MHz	BUK9M20-40H	N/A	N/A
24 V	455 kHz	BUK9K35-60E	BUK9K12-60E	

The VPRE switching slew rate can be configured by I2C to align with an external MOSFET selection and VPRE switching frequency, and to optimize power dissipation and EMC performance. A high slew rate is configured by OTP and can be reduced later by I2C if needed. FS86 uses the current source to drive the external MOSFET so adding an external serial resistor with the gate will not affect the slew rate. To change the slew rate, change the current source selection by I2C.

VPRE MOSFET switching time can be estimated by $T_{SW} = (Q_{GD} + Q_{GS} / 2) / I_{PRE\_GATE\_DRV}$ using the gate charge definition from Figure 16. Q_{GD} and Q_{GS} can be extracted from the MOSFET data sheet.

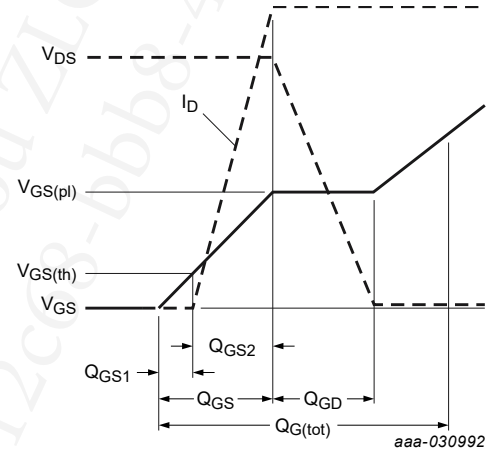


Figure 16. MOSFET gate charge definition

22.9 VPRE efficiency

VPRE efficiency versus current load measurement at the application level is given in Figure 17 and Figure 18 for information with battery voltage VBAT equals to 6.0 V, 14

V and 36 V (455 KHz only), VPRE equals to 3.3 V, based on external components and configuration listed. If the conditions change, the new efficiency can be calculated with the FS86 GUI POWER tool.

Fpre	455	kHz
Cbat	47	µF
ESR Cbat	30	mΩ
Cout_pre	88	µF
ESR Cout_pre	1	mΩ
Lpre	6.8	µH
DCR Lpre	7.1	mΩ
Rshunt	10	mΩ
HS	BUK9M9R5-40H	
LS	BUK9M3R3-40H	
HS_Igate	520	mA
LS_Igate	900	mA

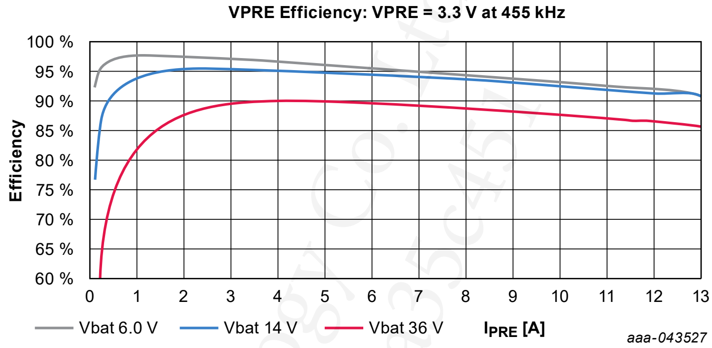


Figure 17. VPRE efficiency at 455 kHz

Fpre	2.22	MHz
Cbat	47	µF
ESR Cbat	30	mΩ
Cout_pre	44	µF
ESR Cout_pre	2	mΩ
Lpre	2.2	µH
DCR Lpre	7.4	mΩ
Rshunt	10	mΩ
HS	BUK7M20-40H	
LS	BUK7M20-40H	
HS_Igate	520	mA
LS_Igate	900	mA

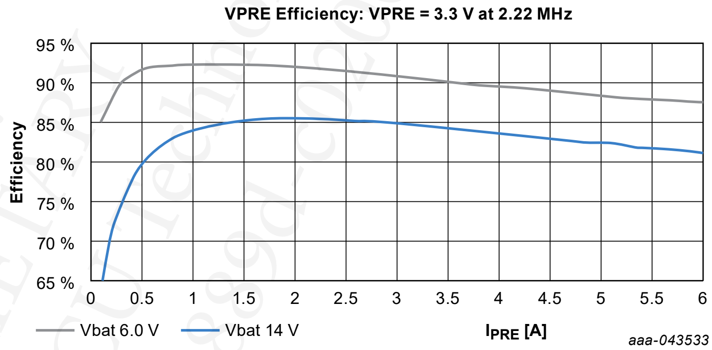


Figure 18. VPRE efficiency at 2.22 MHz

22.10 VPRE protection

An optional protection to open the battery line in case of VPRE High Side MOS Q_{HS} short or leakage is implemented in FS86. The PMOS (MOSFET type-P) Q_{BAT} and driver circuit can be added to disconnect the VPRE circuitry from VSUP. The PMOS Q_{BAT} closure and opening is controlled by the pin BAT_SW. This feature is enabled by OTP (disabled by default).

During the power-up phase, the PMOS Q_{BAT} is closed T_{BAT_SW} (1 ms or 100 ms) before VPRE is enabled. The default timing is configurable using TBAT_SW_CFG OTP bit. The OTP configuration can be inversed by I2C for the next wake up if M_FLAG register TBAT_SW_CFG bit is set to 1.

If PRE_SW pin voltage goes higher than $V_{PRE\_SW\_OV}$ before VPRE is enabled, the device abort the start-up sequence, turn-OFF the PMOS Q_{BAT} and goes DEEP-FS. The same reaction is produced if VPRE goes higher than the ratiometric (+19%) overvoltage $V_{PRE\_FB\_OV}$ at any moment.

The PMOS turn-off event is latched and maintains the PMOS open until DEEP-FS exits to avoid cyclic OV stress.

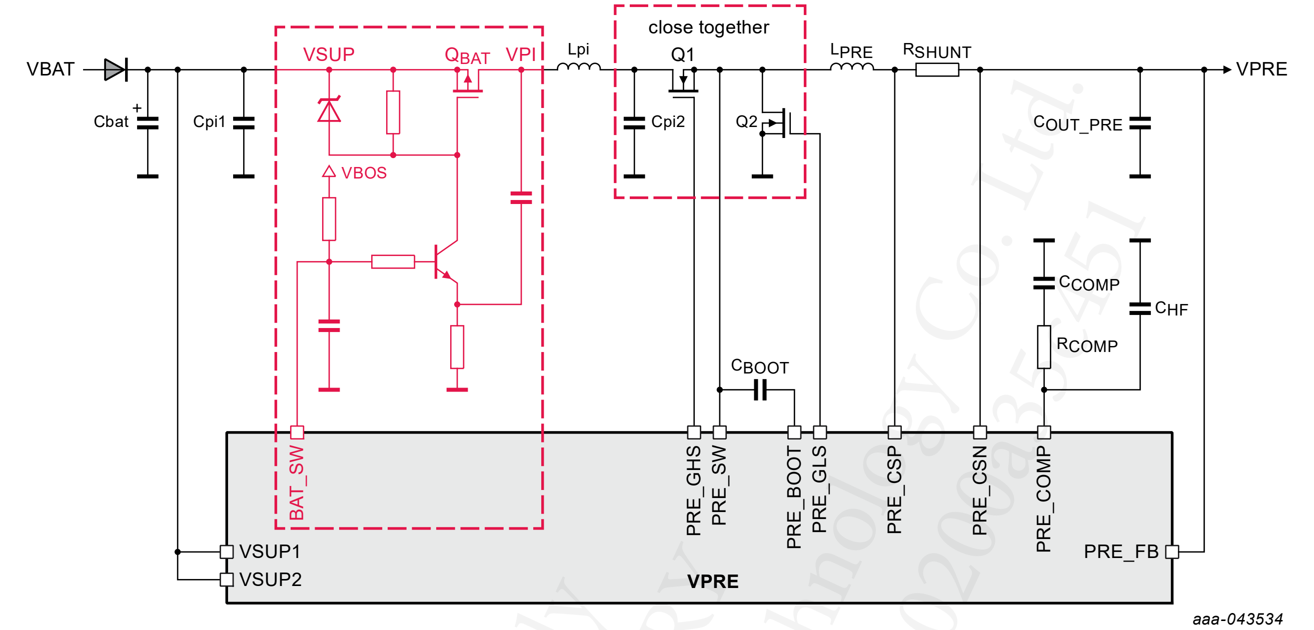


Figure 19. Battery switch protection scheme

The closure timing depends on external components. See the FS86 application note for other scheme examples.

If VPRE high side short protection is disabled by OTP, the BAT_SW pin can be controlled by I2C for release and assertion (to use this open drain output to enable/disable an external IC, for example). Note that the I2C commands can also assert BAT_SW when the portection feature is used, so the functionality can be tested on the fly. It should be noted as well that this will turn-OFF the VPRE supply and consequently send device to STANDBY state/mode.

22.11 VPRE not populated

When two FS86 are used, only one VPRE may be required (VPRE1). It is possible to not populate the external components of the second VPRE (VPRE2) to optimize the bill of material.

In that case, specific VPRE2 pin connections are required:

- PRE_FB2, PRE_CSP2, PRE_CSN2 must be connected to PRE_FB1;
- PRE_COMP2 must be left open;
- PRE_SW2 must be connected to GND;
- PRE_BOOT2 must be connected to VBOS2;
- PRE_GHS2 and PRE_GLS2 must be left open.

After the startup phase, VPRE2 must be disabled by using I2C commands to VPRE_DIS bit.

23 BUCK: Low voltage buck regulator

23.1 Functional description

The BUCK block is a low voltage, synchronous, peak current mode buck converter with integrated HS PMOS and LS NMOS. BUCK works in force PWM and the output voltage is configurable by OTP from 1.0 V to 3.3 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of this block is connected externally to the output of VPRE. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, BUCK switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

An overcurrent detection and a thermal shutdown are implemented on BUCK to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that can lead to the output voltage gradually dropping, causing an undervoltage condition.

BUCK is part number dependent according to OTP BUCK_EN bit. The ramp up and ramp down of BUCK when it is enabled and disabled is configurable with OTP BUCK_DVS[1:0] bits to accommodate multiple MCU soft start requirements.

Programmable phase shift control is implemented (see Section 30.2 "Phase shifting").

23.2 Application schematic

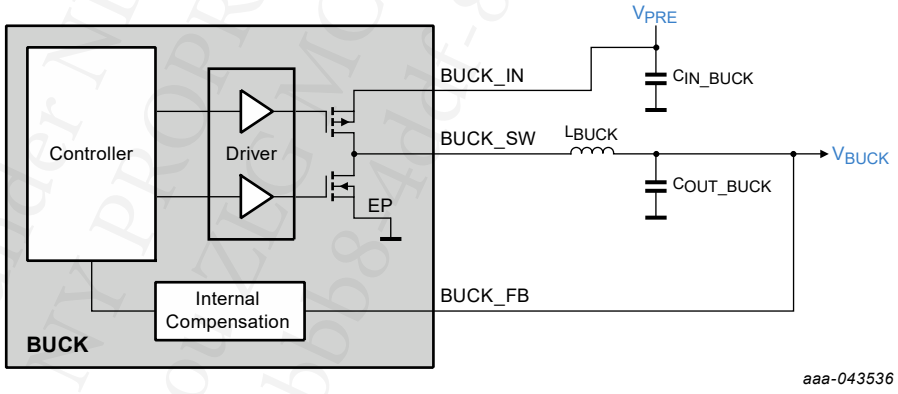


Figure 20. BUCK application scheme

23.3 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. OTP BUCKINDOPT[1:0] scales the slope compensation and the zero cross detection according to the inductor value. 1.0 µH is the recommended inductor value for BUCK.

Use case with V_{PRE} = 3.3 V, V_{BUCK} = 2.3 V, L_{BUCK} = 1.0 µH, F_{BUCK_SW} = 2.22 MHz, C_{OUT_BUCK} = 44 µF.

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

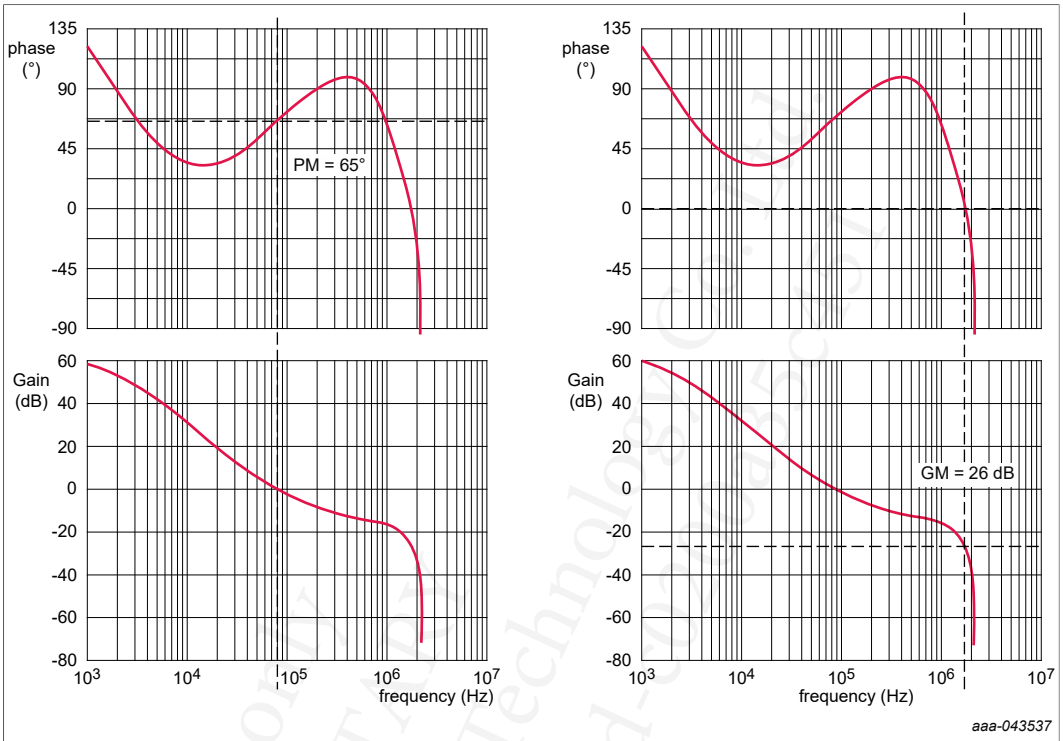


Figure 21. Phase and gain margin simulation

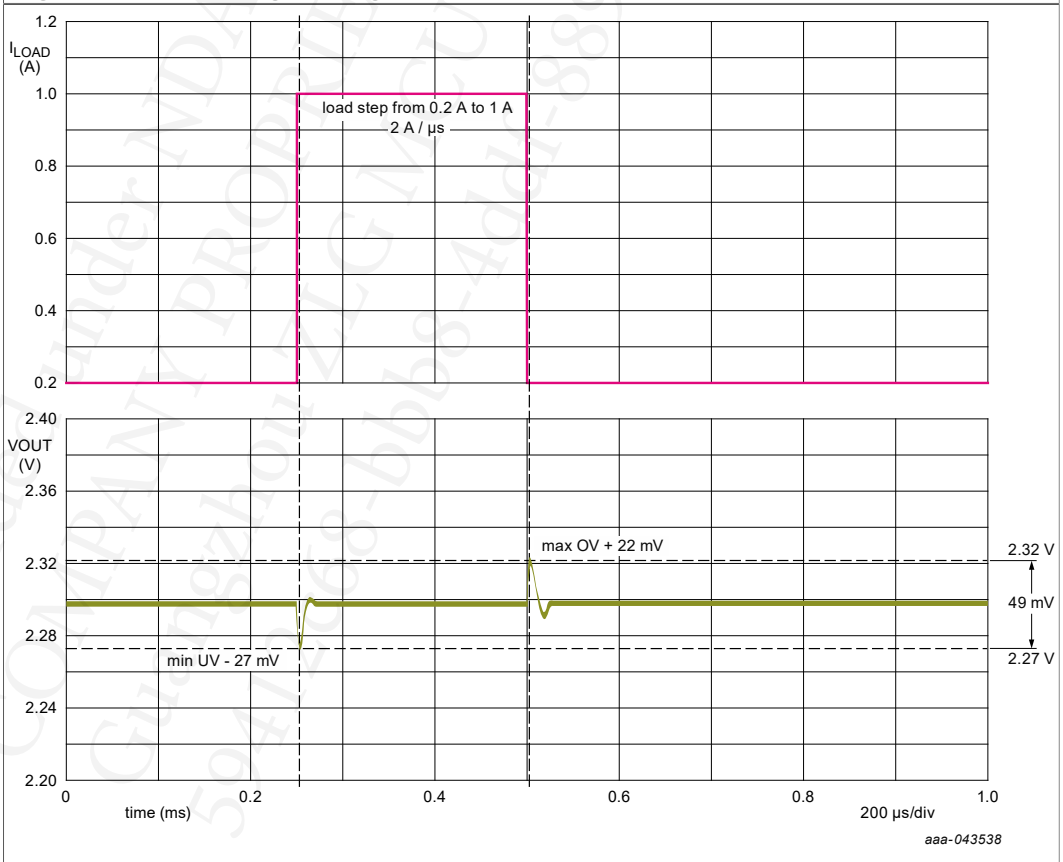


Figure 22. Transient response simulation

23.4 Electrical characteristics

Table 127. Buck electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
BUCK Static Electrical Characteristics					
V_{BUCK_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK}	Output voltage (OTP configurable) 1.0 V, 1.1 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.5 V, 1.6 V, 1.8 V, 1.85 V, 2.0 V, 2.1 V, 2.15 V, 2.25 V, 2.3 V, 2.4 V, 2.5 V, 2.8 V, 3.15 V, 3.2 V, 3.25 V, 3.3 V	1.0	—	3.3	V
	Accuracy	−2.0	—	2.0	%
I_{BUCK}	DC output current capability	2.5	—	—	A
F_{BUCK_SW}	Switching Frequency Range	2.10	2.22	2.35	MHz
I_{LIM_BUCK}	Inductor peak current limitation range BUCKILIM[1:0] = 00 BUCKILIM[1:0] = 11	 1.6 3.6	 2.1 4.5	 2.5 5.5	A
$T_{BUCK\_ON\_MIN}$	HS minimum ON time	5.0	50	80	ns
$V_{BUCK\_DVS\_UP\_DOWN}$	Ramp up and ramp down speed OTP BUCK_DVS[1:0] = 00 OTP BUCK_DVS[1:0] = 01 OTP BUCK_DVS[1:0] = 10 OTP BUCK_DVS[1:0] = 11	 7.81 2.60 1.95 1.56	 10.4 3.47 2.60 2.08	 13.0 4.34 3.26 2.60	mV/µs
$T_{BUCK\_SOFT\_START}$	Soft start time V_{BUCK} = 1.8 V and OTP BUCK_DVS[1:0] = 00 V_{BUCK} = 1.8 V and OTP BUCK_DVS[1:0] = 11 $T_{BUCK\_SOFT\_START}$ = V_{BUCK} / $V_{BUCK\_DVS\_UP\_DOWN}$ To be recalculated for different V_{BUCK} and $V_{BUCK\_DVS\_UP\_DOWN}$	 138 692	 173 865	 230 1154	µs
T_{BUCK_DT}	Dead time to avoid cross conduction	0.01	3.0	20	ns
T_{BUCK_slew}	Slewing Time (10% to 90%, V_{BUCK_IN} = 5.5 V)	1.0	—	5.0	ns
$R_{BUCK\_HS\_RON}$	HS ON resistance	—	—	135	mΩ
$R_{BUCK\_LS\_RON}$	LS ON resistance	—	—	80	mΩ
R_{DIS}	Discharge resistance when disabled	250	500	1000	Ω
TSD_{BUCK}	Thermal shutdown threshold	160	—	—	°C
TSD_{BUCK_HYST}	Thermal shutdown threshold hysteresis	—	9.0	—	°C
T_{BUCK_TSD}	Thermal shutdown filtering time	3.0	5.0	8.0	µs
External components and transient response					
L_{BUCK}	Nominal inductor value (± 30%)	0.47	1.0	1.5	µH
C_{OUT_BUCK}	Effective output capacitor	35	44	120	µF

Table 127. Buck electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN_BUCK}	Nominal input capacitor (low ESR/ESL, close to BUCK_IN pin)	—	4.7	—	µF
	Input decoupling capacitor (close to BUCK_IN pin)	—	0.1	—	µF
$V_{BUCK\_STARTUP}$	Overshoot at startup	—	—	50	mV
V_{BUCK_TLR}	Transient Load Regulation (V_{BUCK_IN} = 2.7 V min, V_{BUCK_FB} = 1.8 V) (Cout = 44 µF, from 200 mA to 1 A, di/dt = 2 A/µs)	−50	—	50	mV

23.5 BUCK efficiency

BUCK efficiency versus current load is given for information based on external component criteria provided and VPRE voltage 4.1 V. If the conditions change, BUCK efficiency vs. current load must be recalculated with the FS86 GUI POWER tool. The real efficiency must be verified by measurement at the application level.

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	20	mΩ
Int. MOSFETs		
HS_Rdson	135	mΩ
QHS	0.5	nC
THS_sw	3	ns
GHS_drive	5	V
LS_Rdson	80	mΩ
QLS	0.5	nC
TLS_sw	3	ns
GLS_drive	5	V

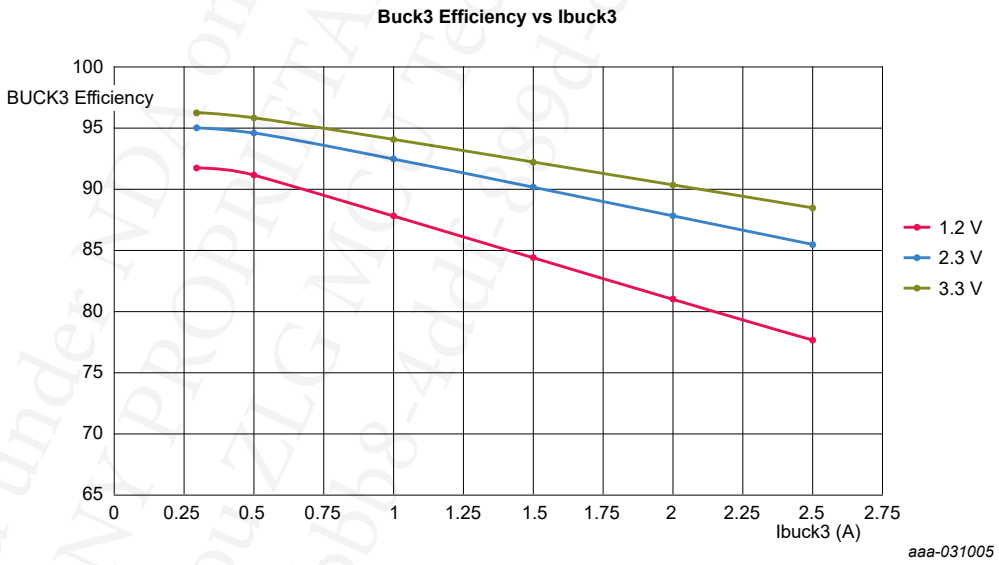


Figure 23. BUCK theoretical efficiency

24 BOOST: Low voltage boost regulator

24.1 Functional description

The BOOST block is a low voltage, nonsynchronous (external diode) rectification, peak current mode boost converter. BOOST works in PWM mode, has an internal low-side FET, and requires an external diode.

BOOST enters skip mode to maintain the correct output voltage in light load condition. The output voltage is configurable by OTP between 5.0 V or and 6.0 V, the switching frequency is 2.22 MHz and the internal low-side FET (input) current is limited to 2.0

A or 3.0 A, depending on OTP configuration. The input of the boost is connected to the output of VPRE. This block is intended to supply LDO1, LDO2 or an external regulator. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, the BOOST switching frequency is derived from the internal oscillator and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I2C.

An overcurrent detection and a thermal shutdown are implemented to protect the internal MOSFET. If an overcurrent is detected after the LS minimum ON-time, the LS is turned OFF and turns ON again at the next BOOST clock rising edge. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on one of the cascaded regulators.

Since the current limitation is on the input current, Table 128 summarizes the expected output current capability depending on VPRE and BOOST voltage configurations and L_{BOOST} = 4.7 µH.

Table 128. Output current capability (LBOOST = 4.7 µH)

VBOOST	VPRE	IBOOST_OUT BOOSTILIM = 01 (2A)	IBOOST_OUT BOOSTILIM = 10 (3A)
5.0 V	2.7 V	0.60 A	0.92 A
	3.3 V	0.77 A	1.17 A
	4.1 V	1.00 A	1.52 A
5.51 V	2.7 V	0.55 A	0.84 A
	3.3 V	0.70 A	1.07 A
	4.1 V	0.90 A	1.38 A
	5.0 V	1.15 A	1.74 A
5.74 V	2.7 V	0.52 A	0.81 A
	3.3 V	0.67 A	1.02 A
	4.1 V	0.87 A	1.32 A
	5.0 V	1.10 A	1.66 A
6.0 V	2.7 V	0.50 A	0.77 A
	3.3 V	0.64 A	0.98 A
	4.1 V	0.83 A	1.26 A
	5.0 V	1.05 A	1.59 A

An overvoltage protection is implemented on BOOST_LS pin. When V_{BOOST_OV} is detected during two consecutive turn-ON cycles, BOOST is disabled. An I2C command is required to enable it again. This monitoring is not safety related.

24.2 Application schematic

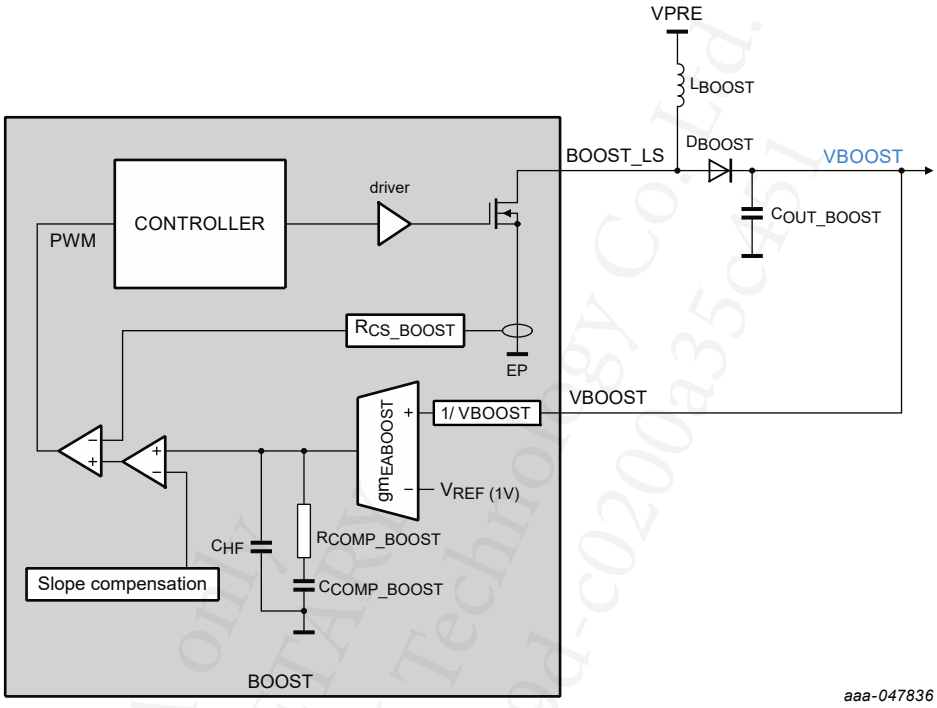


Figure 24. BOOST application scheme

Select a Schottky diode for D_{BOOST} to limit the impact on the SMPS efficiency.

24.3 Compensation network and stability

The internal compensation network, made with R_{COMP}, C_{COMP} and C_{HF} is optimized for best compromise between stability and transient response with R_{COMP} = 750 kΩ, C_{COMP} = 125 pF and C_{HF} = 2.0 pF.

Two BOOST use cases with IBOOST_LIM equals to 2A and 3A are shown in Table 129. Case "a": light load, case "b": full load, case"c": full load during V_{PRE} transient (minimum value).

Table 129. BOOST use case and stability verification

Use case	2a	2b	2c	3a	3b	3c
ILIM_BOOST	2 A			3 A		
VPRE	4.1 V	4.1 V	2.7 V	4.1 V	4.1 V	2.7 V
VBOOST	5.74 V			5.74 V		
LBOOST	4.7 uH			2.2 uH		
COUT_BOOST	22 uF			22 uF		
RBOOST_Rcomp	750 kΩ			750 kΩ		
CBOOST_Ccomp	125 pF			125 pF		
VBOOST_SLOPE	135 mV/µs			178 mV/µs		
ILOAD	10 mA	400 mA	400 mA	20 mA	800 mA	800 mA

Table 129. BOOST use case and stability verification*...continued*

Use case	2a	2b	2c	3a	3b	3c
Phase Margin	70.8°	73.7°	72.8°	74.8°	70.9°	72.9°
Gain Crossover Frequency	5.67 kHz	16.9 kHz	9.40 kHz	8.34 kHz	24.4 kHz	12.5 kHz
Gain Margin	-	20.0 dB	16.7 dB	-	17.1 dB	13.4 dB

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

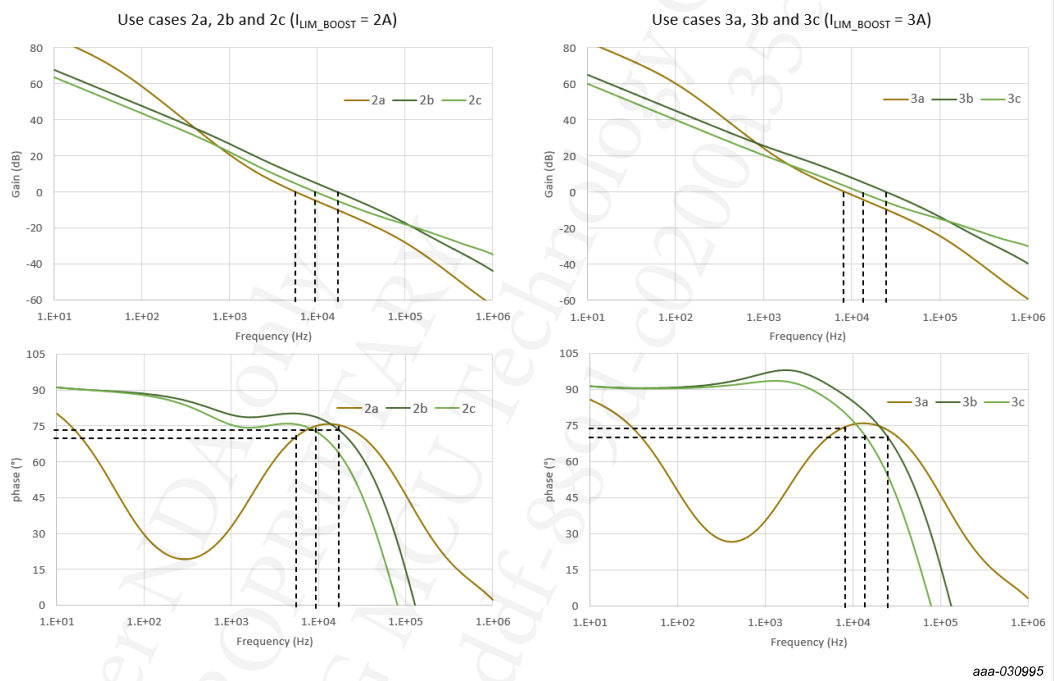


Figure 25. BOOST phase and gain margin simulation

Use case transient response verification:

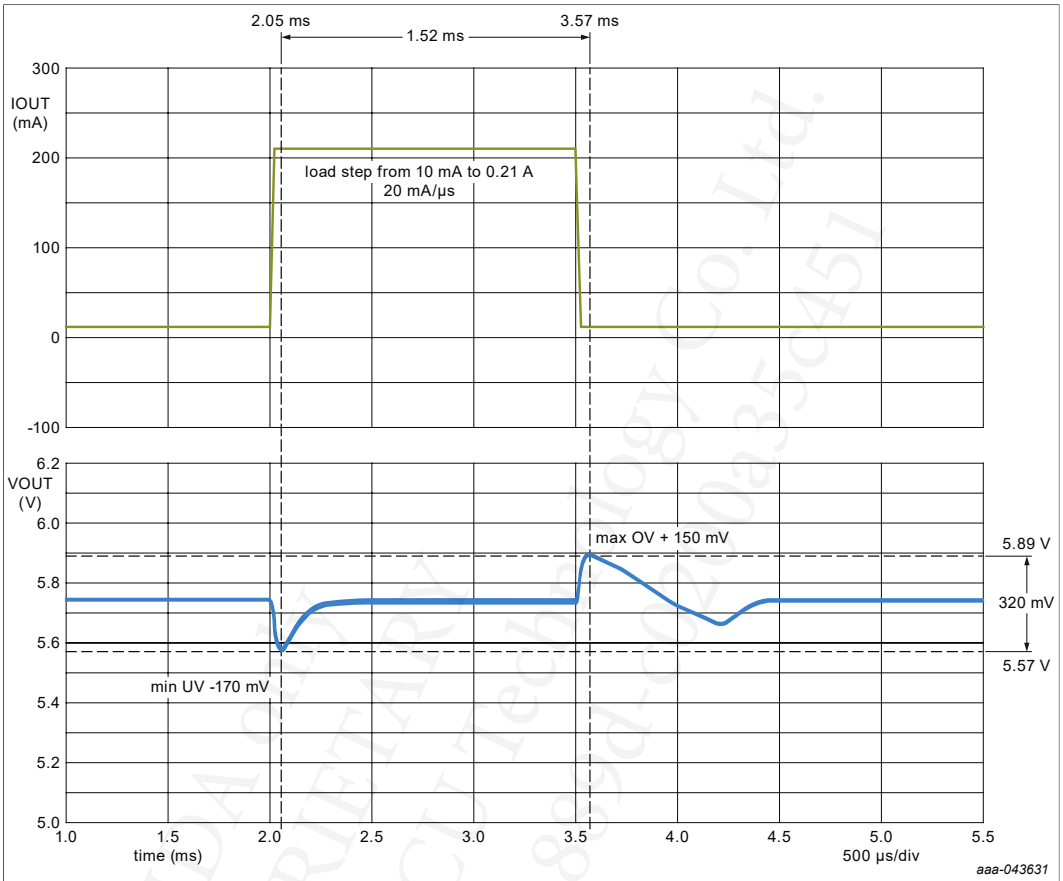


Figure 26. BOOST transient response simulation

24.4 Electrical characteristics

Table 130. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VBOOST					
V_{BOOST}	Output voltage				V
	OTP BOOSTV[3:0] = 0110	4.85	5.00	5.15	
	OTP BOOSTV[3:0] = 0111	4.94	5.09	5.24	
	OTP BOOSTV[3:0] = 1000	5.03	5.19	5.35	
	OTP BOOSTV[3:0] = 1001	5.13	5.29	5.45	
	OTP BOOSTV[3:0] = 1010	5.24	5.40	5.56	
	OTP BOOSTV[3:0] = 1011	5.35	5.51	5.68	
	OTP BOOSTV[3:0] = 1100	5.46	5.63	5.80	
	OTP BOOSTV[3:0] = 1101	5.57	5.74	5.91	
	OTP BOOSTV[3:0] = 1110	5.69	5.87	6.05	
	OTP BOOSTV[3:0] = 1111	5.82	6.00	6.18	
$T_{BOOST\_SOFT\_START}$	Soft start (from enable to 90%)	250	500	750	µs
	DAC soft start completion	—	—	825	µs

Table 130. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{BOOST_OSH}	Start-up Overshoot			3.0	%
V_{BOOST_OV}	Over voltage protection threshold	7.4	—	7.9	V
F_{BOOST_SW}	Switching Frequency Range	2.10	2.22	2.35	MHz
L_{BOOST}	Nominal inductor value	2.2	4.7	6.8	uH
C_{OUT_BOOST}	Effective output capacitor	16	-	66	uF
$V_{BOOST\_LOAD\_REG}$	Transient load regulation (C_{OUT_BOOST} = 20 uF, di/dt = 200 mA/us) from 10 mA to 400 mA	—	—	750	mV
	(C_{OUT_BOOST} = 20 µF, di/dt = 200 mA/µs) from 1 mA to 20 mA	—	—	500	
$V_{BOOST\_LS\_SR}$	Slew Rate of the switching output BOOSTSR[1:0] = 10 BOOSTSR[1:0] = 11	 — —	 300 500	 750 1500	V/µs
I_{LIM_BOOST}	Inductor peak current limitation range OTP BOOSTILIM = 01 OTP BOOSTILIM = 10	 1.50 2.25	 2.00 3.00	 2.75 3.75	A
R_{CS_BOOST}	LS current sense gain OTP BOOSTILIM = 01 (2A) OTP BOOSTILIM = 10 (3A)	 170 115	 233 155	 285 190	mΩ
$T_{BOOST\_ON\_MIN}$	LS minimum ON time OTP BOOSTONTIME = 00 OTP BOOSTONTIME = 01 OTP BOOSTONTIME = 10 OTP BOOSTONTIME = 11	 40 30 50 60	 60 50 70 80	 90 80 100 120	ns
R_{BOOST_RON}	LS ON resistance OTP BOOSTILIM = 01 OTP BOOSTILIM = 10	 — —	 150 125	 280 220	mΩ
$gm_{EABOOST}$	BOOST Error amplifier transconductance	4.5	7.0	8.0	µS
R_{BOOST_Rcomp}	BOOST R compensation value OTP BOOSTCOMP[1:0] = 00 OTP BOOSTCOMP[1:0] = 01	 500 250	 750 500	 900 1000	kΩ
C_{BOOST_Ccomp}	BOOST C compensation value OTP BOOSTCOMP[1:0] = 00	 90	 125	 175	pF
	BOOST slope compensation				

Table 130. Electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{BOOST_SLOPE}	OTP BOOSTSC[4:0] = 00010	200	358	500	mV/µs
	OTP BOOSTSC[4:0] = 01001	180	315	420	
	OTP BOOSTSC[4:0] = 00100	150	257	350	
	OTP BOOSTSC[4:0] = 00011	150	253	350	
	OTP BOOSTSC[4:0] = 00101	110	198	270	
	OTP BOOSTSC[4:0] = 01010	100	178	250	
	OTP BOOSTSC[4:0] = 00110	90	160	230	
	OTP BOOSTSC[4:0] = 11001	80	155	220	
	OTP BOOSTSC[4:0] = 00111	70	135	190	
	OTP BOOSTSC[4:0] = 01100	70	125	190	
	OTP BOOSTSC[4:0] = 01101	50	98	140	
	OTP BOOSTSC[4:0] = 11010	45	90	125	
	OTP BOOSTSC[4:0] = 01110	40	79	110	
	OTP BOOSTSC[4:0] = 01111	35	67	95	
	OTP BOOSTSC[4:0] = 11100	35	63	95	
	OTP BOOSTSC[4:0] = 11101	25	49	70	
	OTP BOOSTSC[4:0] = 11110	20	40	60	
	OTP BOOSTSC[4:0] = 11111	15	33	45	
TSD_{BOOST}	Thermal shutdown threshold	160	—	—	°C
TSD_{BOOST_HYST}	Thermal shutdown threshold hysteresis	—	9.0	—	°C
T_{BOOST_TSD}	Thermal shutdown filtering time	3.0	5.0	8.0	µs

24.5 BOOST not populated

It is possible to not use the BOOST when VPRE is configured at 5.0 V. In this case, the external BOOST components can be unpopulated to optimize the bill of material. The OTP BOOSTEN bit must be programmed to 0 and VBOOST pin must be connected to VPRE. BOOST_LS pin must be left open.

BOOST must be used when VPRE is configured between 3.3 V and 4.9 V to supply VBOS.

25 LDO1: Low-dropout regulator 1

25.1 Functional description

LDO1 is a linear voltage regulator. The output voltage is configurable by OTP from 1.5 V to 5.0 V and its maximum output current is 400 mA.

LDO1 can also be used as load switch to connect a load with minimum input-output drop. This mode is enabled with OTP LDO1_SW_EN bit.

LDO1 input supply is external and can be connected to VPRE, BUCK, BOOST or another supply limited to 5.0 V. An overcurrent detection and a thermal shutdown are implemented on LDO1 to protect the internal pass device.

25.2 Application schematic

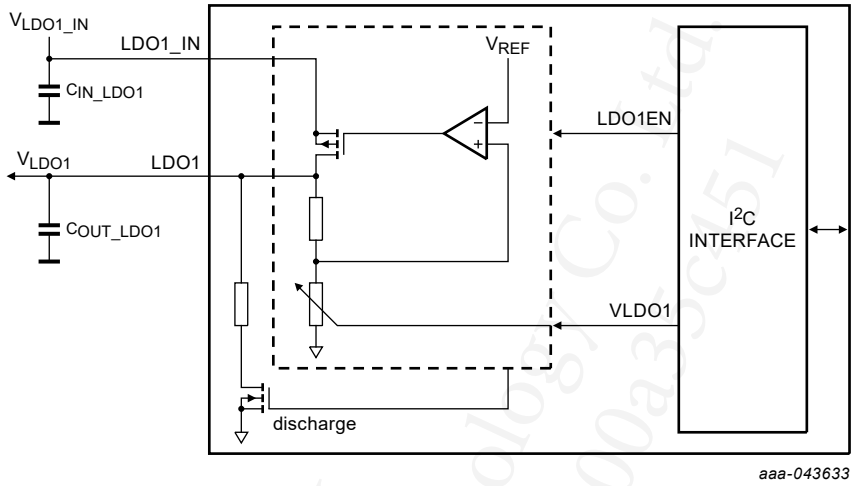


Figure 27. LDO1 application scheme

25.3 Electrical characteristics

Table 131. LDO1 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
LDO1					
V_{LDO1_IN}	Input voltage range	2.5	—	5.5	V
V_{LDO1}	Output voltage (OTP configurable) 1.5 V, 1.6 V, 1.8 V, 1.85 V, 2.15 V, 2.5 V, 2.8 V 3.0 V, 3.1 V, 3.15 V, 3.2 V, 3.3 V, 3.35 V, 4.0 V, 4.9 V, 5.0 V	1.5	—	5.0	V
V_{LDO1_ACC}	Output Voltage accuracy	−3.0	—	3.0	%
V_{LDO1_HR}	Minimum HeadRoom Voltage for 400 mA current capability	0.25	—	—	V
$V_{LDO1\_DO\_mode}$	Maximum voltage between input and output when LDO1 is in dropout mode for 400 mA current	—	—	0.1	V
C_{IN_LDO1}	Nominal input capacitor (close to LDO1_IN pin)	—	1.0	—	µF
C_{OUT_LDO1}	Effective output capacitor	3.3	4.7	6.1	µF
I_{LDO1_ILIM}	Current limitation in LDO mode	450	850	1475	mA
$T_{LDO1\_SOFT\_START}$	Soft start (10% to 90 %)	150	210	280	µs
$V_{LDO1\_STARTUP}$	Overshoot at startup	—	1.0	2.0	%
V_{LDO1_LITR}	Transient Line Response V_{LDO1_IN} = 2.5 V/10 µs (For any 0 mA < I_{LDO1} < 400 mA)	−5.0	—	5.0	%
V_{LDO1_LTR}	Transient Load Regulation (from 10 mA to 200 mA in 2 µs)	−6.0	—	6.0	%

Table 131. LDO1 electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO1_noise}	Output Noise Voltage V_{LDO1_IN} = 2.5 V, V_{LDO1} = 1.8 V, I_{LDO1} = 10 mA 100 Hz to 100 kHz	30	75	150	µV
R_{DIS}	Discharge resistance when disabled	50	100	300	Ω
TSD_{LDO1}	Thermal shutdown threshold	160	—	—	°C
TSD_{LDO1_HYST}	Thermal shutdown threshold hysteresis	—	9.0	—	°C
T_{LDO1_TSD}	Thermal shutdown filtering time	3.0	5.0	8.0	µs
LDO1 Load Switch mode					
$I_{LDO1\_ILIM\_LS}$	Current limitation in load switch mode	450	1000	2000	mA
R_{LDO1}	Drop-out/load switch on resistance	—	—	220	mΩ
T_{LDO1_ON}	Load switch mode turn-ON rise time	—	150	300	µs

26 LDO2: Low-dropout regulator 2

26.1 Functional description

LDO2 is a linear voltage regulator. The output voltage is configurable by OTP from 1.1 V to 5.0 V. A minimum voltage drop is required depending on the output current capability (0.5 V for 150 mA and 1.0 V for 400 mA). The LDO current capability is linear with the voltage drop and can be estimated to $V_{LDO2\_DROP\_MIN}$ = [I(mA) -100] / 500 for intermediate voltage drop between 0.5 V and 1.0 V.

LDO2 input supply is internally connected to BOOST sense pin BOOST_FB. An overcurrent detection and a thermal shutdown are implemented on LDO2 to protect the internal pass device.

26.2 Application schematic

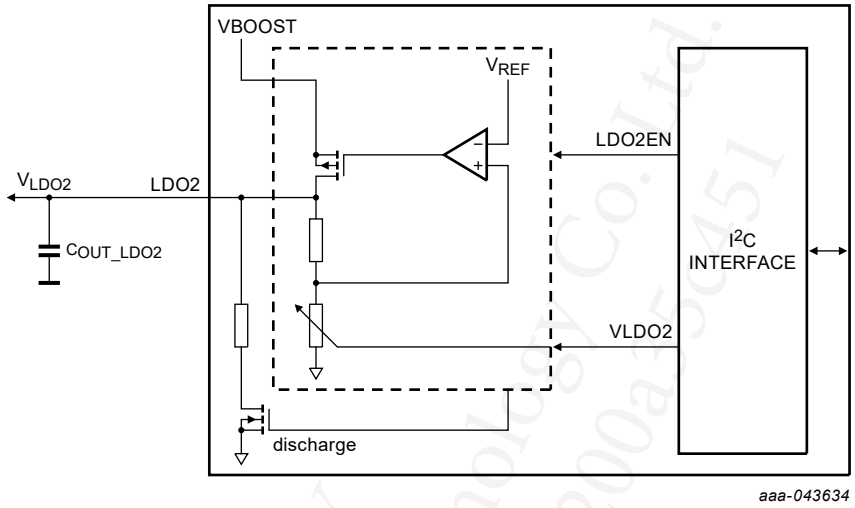


Figure 28. LDO2 application scheme

26.3 Electrical characteristics

Table 132. LDO2 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
LDO2					
V_{LDO2_IN}	Input voltage range	2.5	—	6.5	V
V_{LDO2}	Output voltage (OTP configurable) 1.1 V, 1.2 V, 1.6 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V, 5.0 V	1.1	—	5.0	V
C_{IN_LDO2}	Input capacitor (close to VBOOST pin)	1.0	—	—	µF
C_{OUT_LDO2}	Output decoupling capacitor	0.1	—	—	µF
$T_{LDO2\_SOFT\_START}$	Soft start (Enable to 90%)	0.7	1.0	1.3	ms
$V_{LDO2\_STARTUP}$	Overshoot at startup	—	—	2.0	%
R_{LDO2_DIS}	Discharge resistance when disabled	10	20	60	Ω
TSD_{LDO2}	Thermal shutdown threshold	160	—	—	°C
TSD_{LDO2_HYST}	Thermal shutdown threshold hysteresis	—	9.0	—	°C
T_{LDO2_TSD}	Thermal shutdown filtering time	3.0	5.0	8.0	µs
I_{LDO2_ILIM}	Current limitation OTP LDO2ILIM = 0 (400 mA current capability) OTP LDO2ILIM = 1 (150 mA current capability)	 450 200	 560 280	 800 500	mA
TSD_{LDO2}	Thermal shutdown threshold	160	—	—	°C
TSD_{LDO2_HYST}	Thermal shutdown threshold hysteresis	—	9.0	—	°C
T_{LDO2_TSD}	Thermal shutdown filtering time	3.0	5.0	8.0	µs
OTP LDO2ILIM = 1 (150 mA current capability)					

Table 132. LDO2 electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. V_{SUP} = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$C_{OUT\_LDO2\_150}$	Effective output capacitor, 150 mA current capability	3.0	4.7	13	µF
$V_{LDO2\_ACC\_150}$	Output Voltage accuracy, 150 mA current capability	−2.0	—	2.0	%
$V_{LDO2\_HR\_150}$	Minimum HeadRoom Voltage for 150 mA current capability	0.5	—	—	V
$V_{LDO12\_DO\_mode\_150}$	Maximum voltage between input and output when LDO is in dropout mode for 150 mA current	—	—	0.3	V
$V_{LDO2\_LTR\_150}$	Transient Load Regulation (from 10 mA to 150 mA in 2 µs)	−4.0	—	4.0	%
OTP LDO2ILIM = 0 (400 mA current capability)					
$C_{OUT\_LDO2\_400}$	Effective output capacitor, 400 mA current capability	4.5	10	13	µF
$V_{LDO2\_ACC\_400}$	Output Voltage accuracy, 400 mA current capability	−3.0	—	3.0	%
$V_{LDO2\_HR\_400}$	Minimum HeadRoom Voltage for 400 mA current capability	1.0	—	-	V
$V_{LDO12\_DO\_mode\_400}$	Maximum voltage between input and output when LDO is in dropout mode for 400 mA current	—	—	0.8	V
$V_{LDO2\_LTR\_400}$	Transient Load Regulation (from 10 mA to 400 mA in 4 µs)	−5.0	—	5.0	%
$I_{LDO2\_ILIM\_400}$	Current limitation, current capability (LDO2ILIM = 0)	450	560	800	mA

27 XFAILB: Power synchronization

The power-up and power-down sequence can be synchronized with NXP low voltage PMIC (PF50 series for example) and/or with another FS86 using the XFAILB pin. The synchronization is made using OTP XFAILB_CFG[1:0] register shown in Table 133

Table 133. XFAILB configuration

XFAILB_CFG[1:0]	XFAILB synchronization configuration
00	No synchronization
01	Wait for XFAILB release in a slot (OTP XFAILBS[3:0]) (Synchronization low voltage PMIC)
10	Wait for XFAILB release before enabling VPRE (twin) (Synchronization of two FS86)
11	Not used / Not allowed

27.1 Synchronization with NXP low voltage PMIC (XFAILB_CFG[1:0] = 01)

When XFAILB is used to synchronize FS86 with NXP low voltage PMICs (like PF50 series), FS86 and low voltage PMICs XFAILB pins must be connected together and pulled up to a FS86 rail (BUCK, LDO1 or LDO2) excluding VPRE and BOOST. The FS86 rail used must start before all low voltage PMICs rails, otherwise the XFAILB pin level will not rise and PMICs power-up sequence will not be executed. An example with FS86 VMON0_I2C and PF50 is shown in Figure 29 .

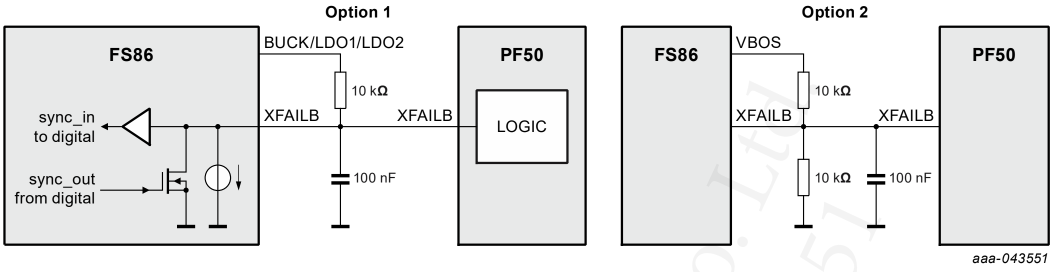


Figure 29. XFAILB connection with a PF50 device

If there is not a compliant rail other than VPRE that starts before all low voltage PMICs rails, connect XFAILB to a symmetric resistor divider connected to VBOS and GND. In this case, a minimum delay of 2 ms must be added at PF devices between XFAILB release and PF's LV regulators start-up. This delay is necessary to prevent PF's from restarting if VPRE is still high when FS86 goes to LPOFF where XFAILB is released. An example is shown in Figure 30 where the 2 ms minimum delay is shown between XFAILB release and PF's LV regulators start-up.

When OTP XFAILB_CFG[1:0] = 01, FS86 Main state machine releases XFAILB in the slot configured in OTP XFAILBS[3:0] register. During the power down sequence, FS86 asserts XFAILB in the same slot by default. However, the slot where XFAILB is asserted during power down sequence can be modified by using I2C on the XFAILBS[3:0] register during NORMAL_M state.

Figure 30 shows the synchronization time diagram between FS86 and the NXP low voltage PMIC PF50. In the timing diagram shown, the FS86 XFAILB is released in SLOT_0, then PF50 manages its own power-up sequence during 12 Tslot periods until SLOT_11, and finally the FS86 starts its low voltage regulators from SLOT_12 to SLOT_14. Once FS86 finishes the start-up sequence, FS86 RSTB and PGOOD are released. The power down sequence starts with a I2C GOTOSTBY command, then FS86 RSTB/PGOOD are asserted and slot reverse execution starts:

- **Solid lines** show the case where XFAILB slot is not changed, i.e. stills in SLOT_0, a delay is added between SLOT_0 and VPRE turn-OFF using OTP VPRE_OFF_DLY = 1 to accommodate PF50 power down sequence;
- **Dotted lines** show the case where XFAILB slot is changed to SLOT_14. As PF50 power-down sequence is finished before SLOT_0 completion, the VPRE turn-OFF delay is not needed (OTP VPRE_OFF_DLY = 0). The power-down is also properly executed when XFAILB is externally asserted (OTP XFAILB_PWD_CFG = 1).

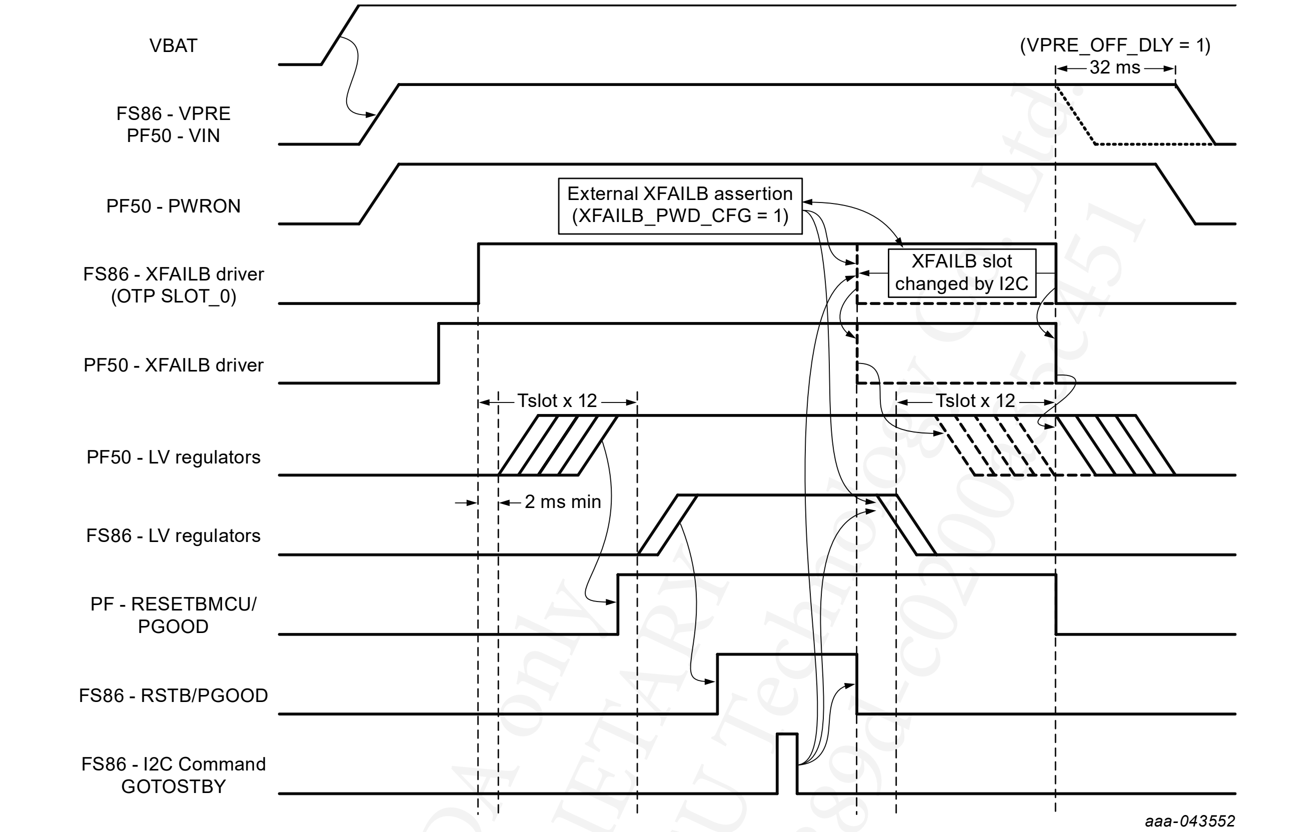


Figure 30. Synchronization of FS86 + NXP low voltage PMIC PF50

During power-up sequence (after VPRE is enabled and before the Main state machine reaches NORMAL_M), FS86 goes to Deep FailSafe mode (DEEP-FS) and waits for WAKE1 OFF/ON cycle or AutoRety timeout (4 s) to restart, if:

- XFAILB is not released externally within $XFAILB_{TIMEOUT}$ (210 ms);
- XFAILB is released, goes high and then is externally asserted.

When in NORMAL_M state, if OTP XFAILB_PWD_CFG = 1 and XFAILB is asserted low externally, FS86 waits for $XFAILB_{TWAIT}$ (20 µs) and starts its power down sequence.

27.2 Synchronization of two FS86 (XFAILB_CFG[1:0] = 10)

When XFAILB is used to synchronized 2x FS86, XFAILB pins of both FS86 shall be connected together and pulled up with a resistor to VBOS at application level. In this case, both FS86 Main state machine stops before VPRE is enabled and wait for XFAILB release by each FS86 to synchronize the power-up sequence (OTP XFAILB_CFG[1:0] = 10).

When OTP XFAILB_PWD_CFG = 1 and XFAILB is asserted low externally, FS86 waits for $XFAILB_{TWAIT}$ (20 µs) before starting its power down sequence.

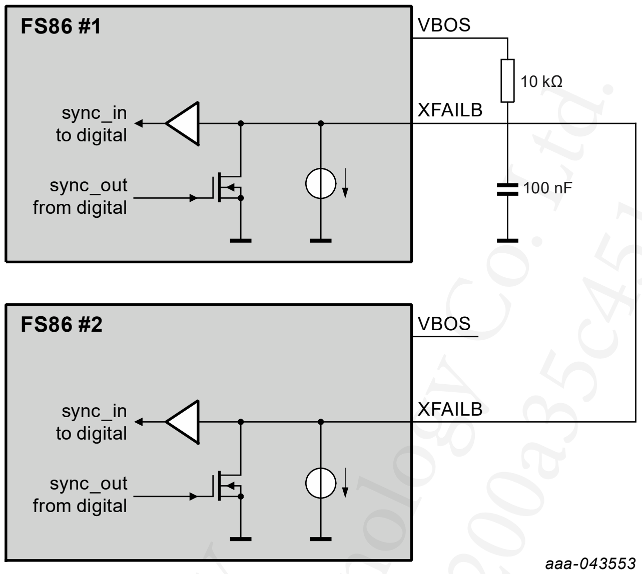


Figure 31. XFAILB connection for synchronization with another PF86 device

27.3 Electrical characteristics

Table 134. XFAILB electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
XFAILB					
$XFAILB_{VIL}$	Low input voltage	0.4	—	—	V
$XFAILB_{VIH}$	High input voltage	—	—	1.4	V
$XFAILB_{HYST}$	Hysteresis	0.1	—	V	V
$XFAILB_{VOL}$	Low output voltage (I = 4.0 mA)	—	—	0.4	V
$XFAILB_{IPD}$	Internal pulldown current source	7.0	10	13	µA
$XFAILB_{ILIM}$	Current limitation	4.0	—	30	mA
$XFAILB_{TWAIT}$	Wait time	18	20	22	µs
$XFAILB_{TIMEOUT}$	Time out	200	210	220	ms

27.4 Synchronization using FOUT pin

When FOUT is not used to provide the frequency synchronization to another PMIC, FOUT can be configured as a digital output by OTP and released high in any power-up slot to enable an external PMIC. FOUT state can be controlled during run mode by I2C. During the power-down sequence, FS86 asserts FOUT in the same slot by default. However, FOUT power-down slot assertion can be modified during Normal mode by I2C to assert FOUT in another slot to respect the reverse order of the power-up sequence.

28 AMUX: Analog multiplexer

28.1 Functional Description

The AMUX pin delivers 17 analog voltage channels to the MCU ADC input. The voltage channels delivered to the AMUX pin can be selected by I2C. The maximum AMUX output voltage range is VMON0_I2C (1.8 V or 3.3 V). External Rs/Cout components are required for the buffer stability.

28.2 Block diagram

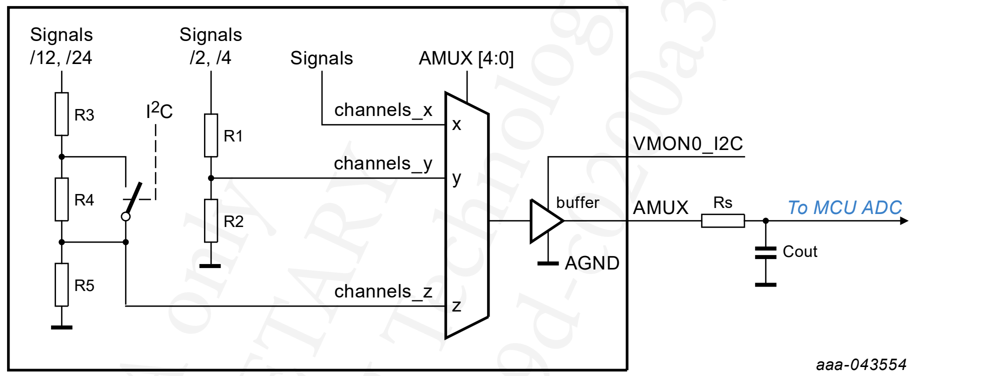


Figure 32. AMUX block diagram

28.3 Channel selection

Table 135. AMUX output selection

AMUX[4:0]	Signal selection for AMUX output
00000	Channel 1: Temperature Sensor $T(°C) = [(V_{AMUX} – V_{TEMP25}) / V_{TEMP\_COEFF}] + 25$
00001	Channel 2: Band Gap Main: 1.0 V ± 1 %
00010	Channel 3: Band Gap Fail Safe: 1.0 V ± 1 %
00011	Channel 4: Vana: 1.6 V ± 2 %
00100	Channel 5: Vdig: 1.6 V ± 2 %
00101	Channel 6: Vdig_FS: 1.6 V ± 2 %
00110	Channel 7: VMON0_I2C voltage (divider 2)
00111	Channel 8: BUCK voltage (divider 2)
01000	Channel 9: VPRE voltage (divider 4)
01001	Channel 10: BOOST voltage (divider 4)
01010	Channel 11: LDO1 voltage (divider 4)
01011	Channel 12: LDO2 voltage (divider 4)
01100	Channel 13: BOS voltage (divider 4)
01101	Channel 14: VSUP (divider selected by RATIO bit)
01110	Channel 15: WAKE1 (divider selected by RATIO bit)

Table 135. AMUX output selection*...continued*

AMUX[4:0]	Signal selection for AMUX output
01111	Channel 16: WAKE2 (divider selected by RATIO bit)
10000	Channel 17: FIN voltage (if OTP PLL_SEL = 0)
10001	Channel 18: Not used
--------	Channel ---: Not used
11111	Channel 32: Not used

FIN can be used as a voltage monitoring input thru the AMUX pin when FIN is not used for frequency input synchronization (when OTP PLL_SEL = 0). In this case, FIN input range is limited to VMON0_I2C operating range since there is no divider on FIN input to the AMUX.

28.4 Electrical characteristics

Table 136. AMUX electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
AMUX					
V_{AMUX_IN}	Input voltage range for VSUP, WAKE1, WAKE2 Ratio 12 (VMON0_I2C = 1.8 V) Ratio 24 (VMON0_I2C = 1.8 V)	 3.6 7.2	 — —	 21 43	V
I_{AMUX}	Output buffer current capability	—	—	2.0	mA
V_{AMUX_OFF}	Offset voltage (Iout = 1 mA)	−7	—	+7	mV
V_{AMUX_RATIO}	Ratio accuracy Ratio 1 Ratio 2 Ratio 4 Ratio 12 Ratio 24	 −0.75 −1.5 −1.5 −1.5 −2.0	 — — — — —	 0.75 1.5 1.5 1.5 2.0	%
V_{TEMP25}	Temperature sensor voltage at 25°C	1.34	1.38	1.42	V
V_{TEMP_COEFF}	Temperature sensor coefficient	−3.8	−3.6	−3.4	mV/°C
T_{AMUX_SET}	Settling time (from 10% to 90% of VMON0_I2C, Rs = 220 Ω, Cout = 10 nF)	—	—	10	µs
Rs	Output resistor	—	220	—	Ω
Cout	Output capacitor	—	10	—	nF

29 I/O interface pins

29.1 WAKE1, WAKE2

WAKE pins are used to manage the internal biasing of the device and main state machine transitions.

- At first start-up, the internal biasing starts regardless of WAKE pins state.
- When the device is in Standby mode and WAKE1 or WAKE2 is > $WAKE12_{VIH}$, the internal biasing is started and the equivalent digital state is '1';
- When WAKE1 or WAKE2 is < $WAKE12_{VIL}$, the equivalent digital state is '0';
- When WAKE1 and WAKE2 are < $WAKE12_{VIL}$, the internal biasing is stopped if the device is in Standby mode (transition to LPOFF state).

WAKE1 and WAKE2 are level based wake-up input signals with analog measurement capability thru AMUX. For example WAKE1 can be connected to a switched VBAT (KL15 line) and WAKE2 to the wake-up output of a CAN or FlexRay transceiver. When a WAKE pin is used as a global pin, a C - R - C protection is required (see Section 32 "Application information").

Table 137. Wake12 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
WAKE1, WAKE2					
$WAKE12_{VIL}$	Digital low input voltage threshold	2.0	—	—	V
$WAKE12_{VIH}$	Digital high input voltage threshold	—	—	2.8	V
I_{WAKE12}	Input current leakage at WAKEx = 36 V	—	—	100	µA
T_{WAKE12}	Filtering time	50	70	100	µs

29.2 INTB

INTB is an open drain output pin with internal pull up to VMON0_I2C. This pin generates a pulse when an internal interrupt occurs to inform the MCU. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in M_INT_MASK registers.

A INTB pulse can be required for diagnosis by the MCU asserting the I2C M_MODE INTB_REQ bit.

Table 138. INTB electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Interrupt pin					
$INTB_{PULL-up}$	Internal pull-up resistor to VMON0_I2C	5.5	10	15	kΩ
$INTB_{VOL}$	Low output level threshold (I = 2.0 mA)	—	—	0.5	V
$INTB_{ILIM}$	INTB current limitation	4.0	—	20	mA
$INTB_{PULSE}$	Pulse duration (without manual frequency tuning)	90	100	110	µs
$INTB_{TDLY}$	Delay between INTB_REQ command reception and INTB pulse start	36	40	44	µs

Table 139. List of interrupts from main logic

Interrupt main	Description
VSUP_UV7	VSUP undervoltage 7.0 V
VSUP_UVH	VSUP undervoltage high
VSUP_UVL	VSUP undervoltage low
VBOS_UVH	VBOS undervoltage high
VPRE_OC	VPRE overcurrent
VPRE_FB_OV	VPRE overvoltage protection
VPRE_UVH	VPRE undervoltage high
BOOST_TSD	BOOST overtemperature shutdown event
VBOOST_OV	BOOST overvoltage
BUCK_TSD	BUCK overtemperature shutdown event
BUCK_OC	BUCK overcurrent
LDO1_TSD	LDO1 overtemperature shutdown event
LDO1_OC	LDO1 overcurrent
LDO2_TSD	LDO2 overtemperature shutdown event
LDO2_OC	LDO2 overcurrent
WAKE1	WAKE1 transition
WAKE2	WAKE2 transition
COM	I2C communication error

Table 140. List of interrupts from Fail-Safe logic

Interrupt fail-safe	Description
FCCU12	FCCU12 bi-stable error detected
FCCU1	FCCU1 single error detected
FCCU2	FCCU2 single error detected
ERRMON	External IC error detected
VMONx_OV	VMONx overvoltage detected (x from 0 to 9)
VMONx_UV	VMONx undervoltage detected (x from 0 to 9)
WD_BAD_DATA	Wrong watchdog refresh – wrong data
WD_BAD_TIMING	Wrong watchdog refresh – CLOSED window or timeout

29.3 BAT_SW

When the battery switch protection is not used (OTP BAT_SW_EN = 0), the BAT_SW pin can be used as General Purpose Output (GPO).

The BAT_SW pin status can be read and manipulated in M_BAT_SW register:

- BAT_SW_SNS bit reports the BAT_SW pad status;
- BAT_SW_DRV bit reports the BAT_SW digital driver command;

- Writing 1 to BAT_SW_ASSERT bit requests BAT_SW pin assertion;
- Writing 1 to BAT_SW_RELEASE bit requests BAT_SW pin release;
- Writing 1 to BAT_SW_ ASSERT and BAT_SW_RELEASE bits together requests BAT_SW pin toggle, i.e. asserts if released, releases if asserted.

If BAT_SW_SNS = 0 and BAT_SW_DRV = 1, BAT_SW pin is forced to 0 externally (open drain output).

Table 141. BAT_SW electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
BAT_SW					
BAT_SW_{VIL}	Low level input voltage	0.7	—	—	V
BAT_SW_{VIH}	High level input voltage	—	—	1.5	V
BAT_SW_{HYST}	Input voltage Hysteresis	100	—	—	mV
BAT_SW_{TFB}	Feedback filtering time	8.0	10	15	µs
BAT_SW_{VOL}	Low level output voltage (I = 2.0 mA)	—	—	0.5	V
BAT_SW_{RPD}	Internal pulldown resistor	1.0	2.0	4.0	MΩ
BAT_SW_{ILIM}	Current limitation	4.0	—	20	mA
BAT_SW_{TFALL}	Fall time • With BAT_SW pull up at VBOS = 5 V • With 10 nF output capacitor to GND • From digital command to assert BAT_SW to BAT_SW_{VIL}	0.2	—	11	µs

30 Clock management

30.1 Description

The clock management block consists of a 20 MHz internal oscillator (default after start up), a Phase Locked Loop (PLL) and multiple dividers. This block manages the clock generation for the internal digital state machines, the switching regulators and the external clock synchronization.

The internal oscillator frequency is programmable by I2C from 16 to 24 MHz in 1 MHz increments in run mode. A triangular and a pseudo random spread spectrum features can be activated and configured by OTP and I2C to reduce the emission of the oscillator fundamental frequency.

The switching regulators can be synchronized with an external frequency coming from the FIN pin. The FIN pin is shared with the VMON9_RES pin, so the FIN pin must be enabled by OTP. A dedicated watchdog monitoring is implemented to verify and report the correct FIN frequency range. Different clocks can be sent to the FOUT pin to synchronize an external IC or for diagnostic purposes. FOUT is configured as a frequency output pin by default but can be also configured by OTP as a digital output (see Section 27.4 "Synchronization using FOUT pin").

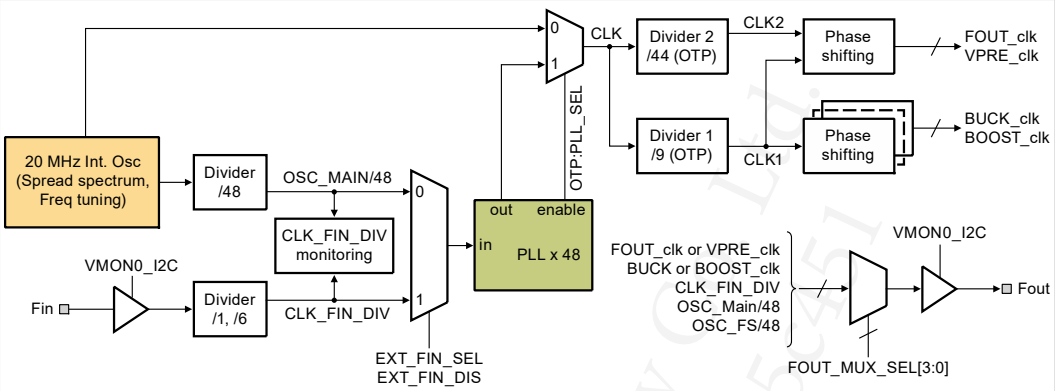


Figure 33. Clock management block diagram

Spread spectrum, frequency tuning or PPL use change the CLK frequency F_{20MHZ} and consequently all timings shown in this document. All timings are specified considering spread spectrum, frequency tuning and PPL disabled (CLK equals to 20 MHz).

30.2 Phase shifting

The clocks of the switching regulators (VPRE_clk, BOOST_clk and BUCK_clk, as well as FOUT) can be delayed in order to prevent all regulators from turning ON at the same time to reduce peak current and improve EMC performance.

Each clock of each regulator can be shifted from 0 to 7 clock cycles of CLK running at 20 MHz, which corresponds to 50 ns. The phase shift configuration is done by OTP configuration using OTP VPRE_PH[2:0], OTP BOOST_PH[2:0], OTP BUCK_PH[2:0] and OTP FOUT_PH[2:0].

VPRE and BUCK have a HS peak current detection architecture. The PWM synchronizes the turn-ON of the high-side switch. BOOST has a LS peak current detection architecture. The PWM synchronizes the turn-ON of the low-side switch.

Table 142. Phase delay configuration

Phase delay code PH[2:0]	Phase delay
000 (default)	no delay
001	1 Main clock period delay
010	2 Main clock periods delay
011	3 Main clock periods delay
100	4 Main clock periods delay
101	5 Main clock periods delay
110	6 Main clock periods delay
111	7 Main clock periods delay

30.3 Manual frequency tuning

The internal oscillator frequency, 20 MHz by default, can be programmed from 16 MHz to 24 MHz in increments of 1.0 MHz frequency by I2C. The oscillator functionality is guaranteed for frequency increments of one step at a time in either direction, with a

minimum of 10 µs between two steps. For any unused code of the CLK_TUNE[3:0] bits, the internal oscillator is set at the default 20 MHz frequency.

To change the internal oscillator frequency from 20 MHz to 24 MHz, four I2C commands are required with 10 µs wait time between each command (21 MHz – wait 10 µs – 22 MHz – wait 10 µs – 23 MHz – wait 10 µs – 24 MHz). To change the internal oscillator frequency from 24 MHz to 16 MHz, eight I2C commands are required with 10 µs wait time between each command (23 MHz – wait 10 µs – 22 MHz – wait 10 µs – 21 MHz – wait 10 µs – 20 MHz – wait 10 µs – 19 MHz – wait 10 µs – 18 MHz – wait 10 µs – 17 MHz – wait 10 µs – 16 MHz).

Table 143. Manual frequency tuning configuration

CLK_TUNE [3:0]	Oscillator frequency
0000 (default)	20 MHz
0001	21 MHz
0010	22 MHz
0011	23 MHz
0100	24 MHz
1001	16 MHz
1010	17 MHz
1011	18 MHz
1100	19 MHz
Reset condition	POR

30.4 Spread spectrum

The internal oscillator can be modulated around the oscillator frequency. The spread spectrum feature can be activated by I2C with the MOD_EN bit and the carrier frequency can be selected by I2C with the MOD_CONF bit. By default, the spread spectrum is disabled. The spread spectrum and the manual frequency tuning functions cannot be used at the same time.

The main purpose of the spread spectrum is to improve the EMC performance by spreading the energy of the internal oscillator and the VPRE frequency on the VBAT frequency spectrum.

For optimal performance, select the triangular spread spectrum when VPRE is configured at 455 kHz and the pseudo random triangular spread spectrum when VPRE is configured at 2.2 MHz.

Table 144. Spread spectrum configuration

MOD_EN	MOD_CONF	Spread spectrum	Manual frequency tuning
0	X	Disabled	YES
1	0	Triangular (19 kHz)	NO
1	1	Pseudo random triangular	NO

30.4.1 Triangular spread spectrum

The triangular spread spectrum is activated in the I2C M_CLCK register by setting the MOD_EN bit high and the MOD_CONF bit low. In this configuration, the internal oscillator is modulated with a triangular carrier frequency of 19 kHz with –10% / 0% deviation range of the nominal oscillator frequency.

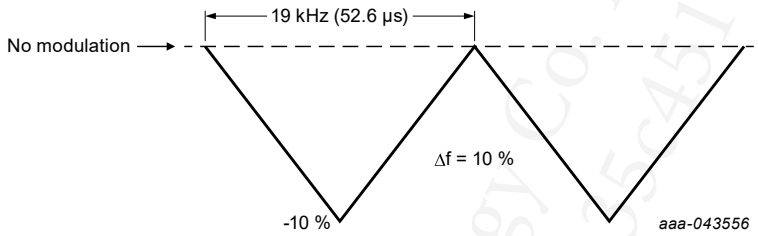


Figure 34. Triangular spread spectrum

30.4.2 Pseudo random triangular spread spectrum

The pseudo random triangular spread spectrum is activated in the M_CLCK I2C register by setting the MOD_EN bit high and the MOD_CONF bit high. In this configuration, the internal oscillator is modulated with a triangular carrier frequency of 19 kHz with –10% / 0% deviation range of the nominal oscillator frequency, but two random commutations on the carrier slope are added in each half period to increase the spectrum spreading.

30.5 External clock synchronization

30.5.1 FIN: Clock input

To synchronize the switching regulators with an external frequency coming from FIN pin, the PLL must be enabled with OTP PLL_SEL bit. The FIN pin accepts two ranges of frequency depending on the divider selection to always have CLK clock at the output of the PLL in the working range of the digital blocks from 16 MHz to 24 MHz. When FIN_DIV = 0, the input frequency range must be between 333 kHz and 500 kHz. When FIN_DIV = 1, the input frequency range must be between 2.0 MHz and 3.0 MHz.

The PLL configuration procedure starts by choosing the FIN clock divider configuration with FIN_DIV bit, then FIN clock can be applied. Finally, the CLK clock can be switched from the internal oscillator to FIN external clock with the EXT_FIN_SEL bit.

If FIN is out of range, CLK clock switches back to the internal oscillator and reports the error using the CLK_FIN_DIV_OK bit. When FIN comes back in the range, the configuration procedure described above must be executed again.

30.5.2 FOUT: Clock output

The FOUT pin can be used to synchronize an external device with the FS86 when OTP FOUT_SLOT_EN is disabled. The frequency sent to FOUT is selected by I2C with the FOUT_MUX_SEL[3:0] bits.

A novel clock can be sent to FOUT when FOUT_clk is chosen in the FOUT_MUX_SEL[3:0] bits. The origin is selected by I2C from CLK1 or CLK2 with FOUT_CLK_SEL bit and its delay is selected with FOUT_PH[2:0].

The FOUT pin can also be used for power synchronization when OTP FOUT_SLOT_EN is enabled. For more information, see Section 27.4 "Synchronization using FOUT pin"

Table 145. FOUT multiplexer selection

FOUT_MUX_SEL[3:0]	FOUT multiplexer selection
0000 (default)	High impedance (HIZ)
0001	VPRE_clk
0010	BOOST_clk
0011	RESERVED
0100	FOUT pin state
0101	BUCK_clk
0110	FOUT_clk
0111	OSC_MAIN/48 (when PLL is enabled by OTP)
1000	OSC_FS/48
1001	CLK_FIN_DIV
Others	No signal, FOUT is low
Reset condition	POR

30.6 Electrical characteristics

Table 146. Clock management electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Internal Oscillator					
F_{20MHz}	Oscillator nominal frequency (I2C programmable)	—	20	—	MHz
F_{20MHz_ACC}	Oscillator accuracy	−6	—	+6	%
T_{20MHz_step}	Oscillator frequency tuning step transition time	—	10	—	µs
Spread spectrum					
FSS_{MOD}	Spread spectrum frequency modulation	—	19	—	kHz
FSS_{RANGE}	Spread spectrum Range	−10	—	0	%
Clock synchronization (FIN)					
V_{FIN_IN}	FIN input voltage range	—	VMON0_ I2C	—	V
DC_{FIN}	FIN duty cycle	40	50	60	%
FIN_{RANGE}	FIN input frequency range (I2C configuration)	333	—	500	kHz
		2.0	—	3.0	MHz
FIN_{VIL}	FIN Low Voltage Threshold	0.3 x VMON0_ I2C	—	—	V

Table 146. Clock management electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
FIN_{VIH}	FIN High Voltage Threshold	—	—	0.7 x VMON0_I2C	V
FIN_{HYST}	FIN hysteresis	0.1	—	—	V
FIN_{PD}	FIN internal pulldown	1	2	4	MΩ
FIN_{DLY}	FIN input buffer propagation delay	—	—	8	ns
FIN_{ERR_FAST}	CLK_FIN_DIV monitoring, fast deviation detection	530	590	650	kHz
FIN_{ERR_SLOW}	CLK_FIN_DIV monitoring, slow deviation detection	200	250	300	kHz
FIN_{TLOST}	Time to switch to internal oscillator when FIN is lost	—	—	3	µs
PLL_{TLOCK}	PLL lock time	—	—	90	µs
PLL_{TSET}	PLL settling time (from EXT_FIN_DIS enable to ±1 % of output frequency)	—	—	125	µs
Clock synchronization (FOUT)					
VF_{OUT_OUT}	FOUT output voltage range	—	VMON0_I2C	—	V
DC_{FOUT}	FOUT duty cycle	40	50	60	%
$FOUT_{VOL}$	FOUT Low Voltage Threshold at 2 mA	—	—	0.5	V
$FOUT_{VOH}$	FOUT High Voltage Threshold at −2 mA	VMON0_I2C −0.5	—	—	V
I_{FOUT}	Tri-state leakage current (VMON0_I2C = 3.3 V)	−0.5	—	0.5	µA
$FOUT_{TRISE}$	FOUT rise time (from 20% to 80% of VMON0_I2C, Cout = 30 pF)	—	—	20	ns
$FOUT_{TFALL}$	FOUT fall time (from 80% to 20% of VMON0_I2C, Cout = 30 pF)	—	—	20	ns

31 Safety

31.1 Functional Description

The Fail-safe domain is electrically independent and physically isolated. The Fail-safe domain is supplied by its own reference voltages and current, has its own oscillator, has duplicated analog path to minimize the common cause failures, and has LBIST/ABIST to cover latent faults.

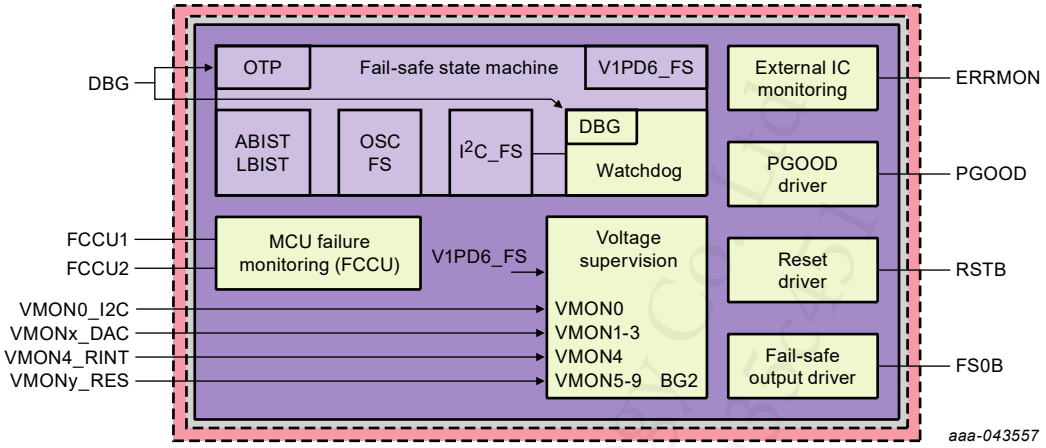


Figure 35. Fail-safe domain block diagram

31.2 ASIL B versus ASIL D

Table 147. Recommended ASIL B vs ASIL D safety features

Safety features	ASIL B	ASIL D
PGOOD output pin	Yes	Yes
RSTB output pin	Yes	Yes
FS0B output pin	Yes	Yes
VMONx_DAC voltage monitoring	Up to 3	Up to 3
VMON0_I2C voltage monitoring	Yes	Yes
VMON4_RINT voltage monitoring	Optional	Optional
VMONy_RES voltage monitoring	Up to 5	Up to 5
Watchdog monitoring	Simple WD	Challenger WD
FCCU monitoring	Optional	Yes
MCU fault recovery strategy	No	Yes
External IC monitoring (ERRMON)	Optional	Yes
Analog BIST (ABIST)	Yes	Yes
Logical BIST (LBIST)	No	Yes

31.3 Fail-safe initialization

After POR or wake up from Standby, when the RSTB pin is released, the Fail-Safe State Machine enters in INIT_FS phase for initialization. To secure the writing process during INIT_FS phase, in addition to CRC computation during I2C transfer, the MCU must perform the following sequence for all INIT_FS registers:

1. Write the desired data in the FS_I_Register_A (DATA)
2. Write the opposite in the FS_I_NOT_Register_A (DATA_NOT)

As an example, if the data of FS_I_Register_A = 0xABCD, the data not of FS_I_NOT_Register_A = 0x5432. A real-time comparison process (XOR) is performed by the FS86 to ensure DATA FS_I_Register_A = DATA_NOT FS_I_NOT_Register_A. Only the utility bits must be inverted in the DATA_NOT content. The RESERVED

bits are not considered and can be written at '0'. If the comparison result is correct, then the REG_CORRUPT is set to '0'. If the comparison result is wrong, then the REG_CORRUPT bit is set to '1'. The REG_CORRUPT monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh.

INIT_FS must be closed by the first good watchdog refresh before **2 seconds** timeout. After INIT_FS closure, it is possible to come back to INIT_FS with the GO_TO_INITFS bit in FS_SAFE_IOS register, from any FS_state after INIT_FS.

31.4 Watchdog

The windowed watchdog is enabled/disabled with OTP WD_DIS bit. The first half of the window is said to be CLOSED and the second half is said to be OPEN. A good watchdog refresh is a good watchdog answer during the OPEN window. A bad watchdog refresh is a bad watchdog answer during the OPEN window, no watchdog refresh during the OPEN window or a good watchdog answer during the CLOSED window. After a good or a bad watchdog refresh, a new window period starts immediately so that the MCU remains synchronized with the windowed watchdog.

Windowed watchdog answer and refresh validation

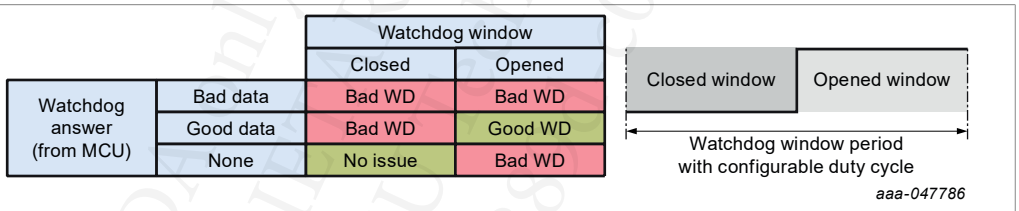


Figure 36. Windowed watchdog answer and refresh validation

The first good watchdog refresh closes the INIT_FS. Then the watchdog window is running and the MCU must refresh the watchdog in the OPEN window of the watchdog window period. The duration of the watchdog window is configurable from 1 ms to > 17 min with the WDW_PERIOD[4:0] bits. The new watchdog window is effective after the next watchdog refresh. The watchdog window can be disabled during INIT_FS only. The watchdog disable is effective when the INIT_FS is closed.

The watchdog configuration must be written first in the FS_WD_WINDOW_DUR and then in the FS_NOT_WD_WINDOW_DUR registers like INIT registers.

Table 148. Watchdog window period configuration

WDW_PERIOD[4:0]	Watchdog Window Period
00000	DISABLE (INFINITE OPEN WINDOW)
00001	1 ms
00010	2 ms
00011 (default)	**3 ms**
00100	4 ms
00101	6 ms
00110	8 ms
00111	12 ms
01000	16 ms
01001	24 ms

Table 148. Watchdog window period configuration*...continued*

WDW_PERIOD[4:0]	Watchdog Window Period
01010	32 ms
01011	64 ms
01100	128 ms
01101	256 ms
01110	512 ms
01111	1024 ms
10000	DISABLE (INFINITE OPEN WINDOW)
10001	1024 ms
10010	2048 ms
10011	3072 ms
10100	4096 ms
10101	6144 ms
10110	8192 ms
10111	12288 ms
11000	16384 ms
11001	24576 ms
11010	32768 ms
11011	65536 ms
11100	131072 ms
11101	262144 ms
11110	524288 ms
11111	1048576 ms
Reset condition	POR

The duty cycle of the watchdog window is configurable from 31.25% to 68.75% with the WDW_DC[2:0] bits. The new duty cycle is effective after the next watchdog refresh.

Table 149. Watchdog window duty cycle configuration

WDW_DC[2:0]	CLOSED window	OPEN window
000	31.25%	68.75%
001	37.5%	62.5%
010 (default)	**50%**	**50%**
011	62.5%	37.5%
100	68.75%	31.25%
Others	50%	50%
Reset condition	POR	

31.4.1 Watchdog selection

Two types of watchdog monitoring can be selected with OTP WD_SELECTION bit.

Table 150. Watchdog type configuration

WD_SELECTION	Watchdog type selection
0	Simple
1	Challenger

The watchdog uses a seed to compute the answer. The seed is stored in the FS_WD_SEED register. Its default value after POR or RSTB assertion is 0x5AB2, but the MCU can send its own seed through I2C.

The MCU must write the answer, through I2C, to the FS_WD_ANSWER register during the OPEN watchdog window. The WD error counter is incremented when the answer is wrong or not given during the open window.

31.4.1.1 Simple Watchdog

The Simple watchdog uses a unique seed. The watchdog answer WD_ANSWER is the seed WD_SEED itself. It is impossible to write 0xFFFF and 0x0000 in FS_WD_SEED register in this configuration. A communication error is reported in case of 0x0000 and 0xFFFF write tentative.

31.4.1.2 Challenger Watchdog

The Challenger watchdog seed changes automatically and the answer has to be computed though a few operations.

A Linear Feedback Shift Register (LFSR) is used to generate a new 16-bits pseudo-random seed at FS_WD_SEED register each time the watchdog is properly refreshed. The MCU can send its own seed during the initialization phase (INIT_FS). It is impossible to write 0x0000 in FS_WD_SEED register. A communication error is reported in case of 0x0000 write tentative.

The answer to be written in FS_WD_ANSWER register has to be calculated using the operations shown in Figure 37 .

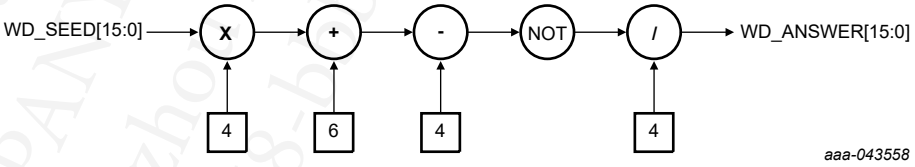


Figure 37. Challenger watchdog answer calculation

31.4.2 Watchdog error counter

The watchdog error counter WD_ERR_CNT[3:0] is implemented in the device to filter out an incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by two. The watchdog error counter is decremented by one each time the watchdog is properly refreshed. This principle ensures a cyclic OK/NOK behavior converges on a failure detection.

To allow flexibility in the application, the maximum value of this counter is configurable with the WD_ERR_LIMIT[1:0] bits during the INIT_FS phase.

Table 151. Watchdog error counter limit configuration

WD_ERR_LIMIT[1:0]	Watchdog error counter limit
00	8
01 (default)	6
10	4
11	2
Reset condition	POR

The watchdog error counter value can be read by the MCU for diagnostic with the WD_ERR_CNT[3:0] bits.

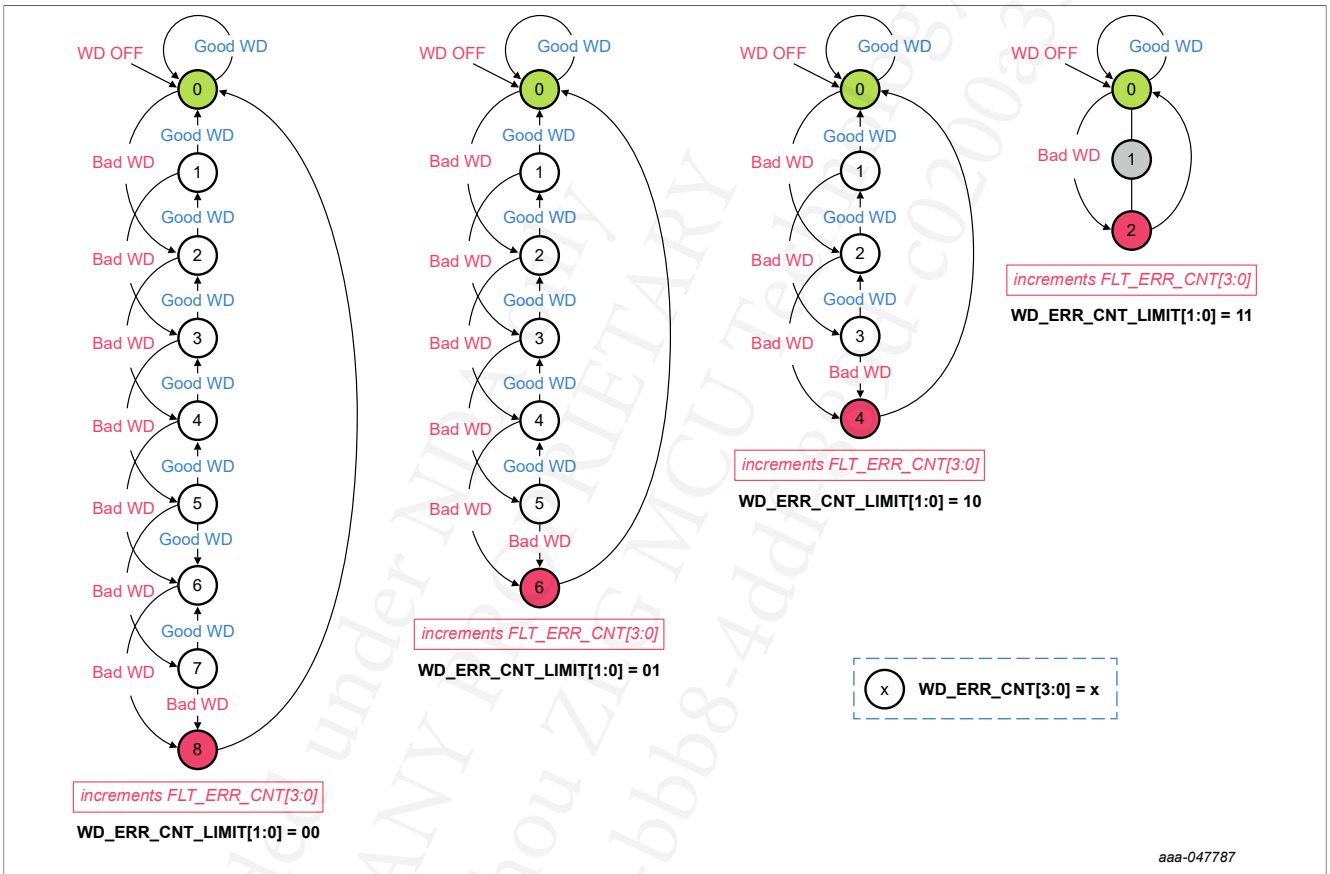


Figure 38. Watchdog error counter configurations

31.4.3 Watchdog refresh counter

The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by one. Each time the watchdog refresh counter reaches its maximum value (six by default) and if the next WD refresh is also good, the fault error counter is decremented by one. Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to zero.

To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable with the WD_RFR_LIMIT[1:0] bits during the INIT_FS phase.

Table 152. Watchdog refresh counter limit configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter limit
00 (default)	**6**
01	4
10	2
11	1
Reset condition	POR

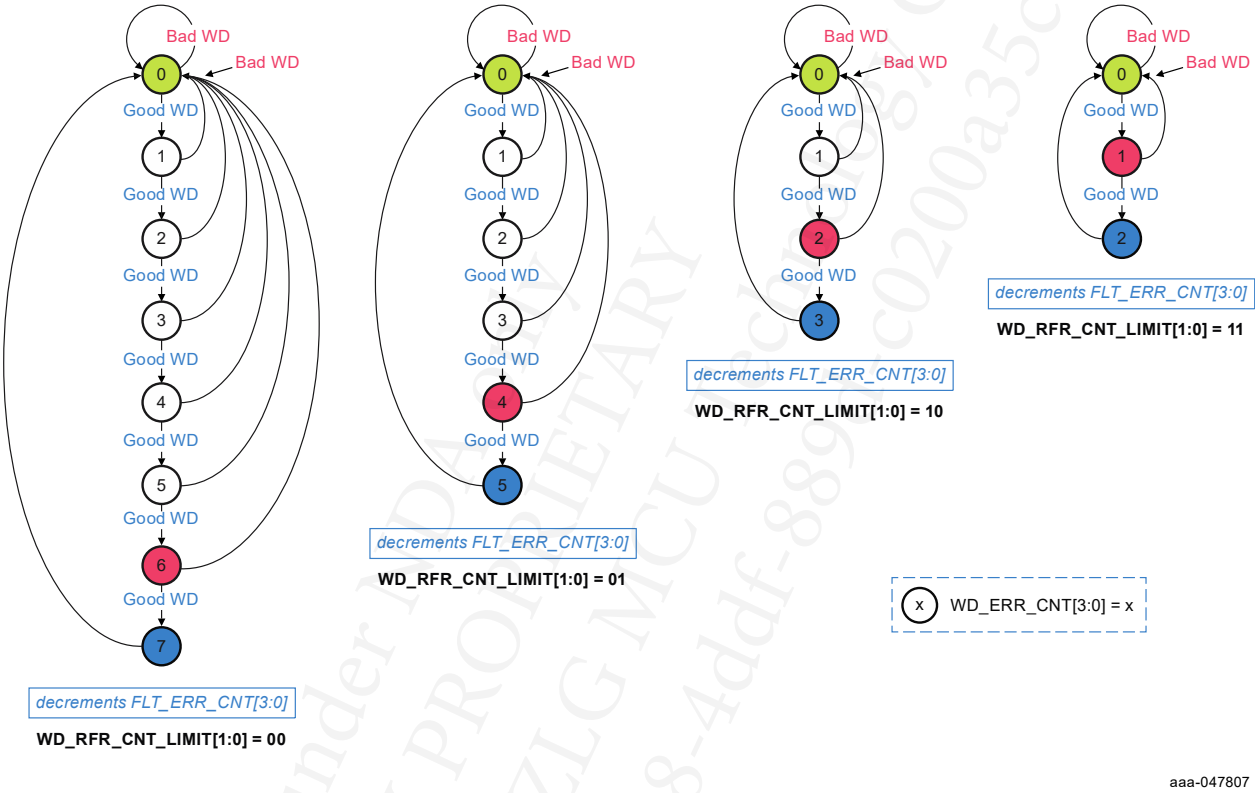


Figure 39. Watchdog refresh counter configurations

31.4.4 Watchdog error impact

When the watchdog error counter WD_ERR_CNT[3:0] reaches its maximum value (watchdog error counter limit), the Fail-safe reaction on RSTB and/or FS0B is configurable with the WD_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 153. Watchdog error impact configuration

WD_FS_IMPACT[1:0]	Watchdog error impact on RSTB/FS0B
00	No action on RSTB and FS0B, WD_ERR_CNT[3:0] has no impact on FLT_ERR_CNT
01	FS0B only is asserted if WD_ERR_CNT[3:0] = watchdog error counter limit (WD_ERR_LIMIT[1:0])
10	**FS0B and RSTB are asserted if WD_ERR_CNT[3:0] = watchdog error counter limit (WD_ERR_LIMIT[1:0])**

Table 153. Watchdog error impact configuration...continued

WD_FS_IMPACT[1:0]	Watchdog error impact on RSTB/FS0B
11	FS0B and RSTB are asserted if WD_ERR_CNT[3:0] = watchdog error counter limit (WD_ERR_LIMIT[1:0])
Reset condition	POR

31.4.5 MCU Fault Recovery Strategy

The Fault Recovery Strategy feature is enabled by OTP FLT_RECOVERY_EN bit. This function extends the watchdog window to allow the MCU to perform a fault recovery strategy. The goal is to not reset the MCU while it is trying to recover the application after a failure event. When a fault is triggered by the MCU via its FCCU pins, the FS0B pin is asserted by the device and the watchdog window duration becomes automatically an open window (no more duty cycle). This open window duration is configurable with the WDW_RECOVERY[3:0] bits during the INIT_FS phase.

Table 154. Watchdog window in fault recovery configuration

WDW_RECOVERY[3:0]	Watchdog Window Duration when the device is in Fault Recovery Strategy
0000	DISABLE
0001	1.0 ms
0010	2.0 ms
0011	3.0 ms
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011(default)	**64 ms**
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

The transition from WDW_PERIOD to WDW_RECOVERY happens when the FCCU pin indicates an error and FS0B is asserted. If the MCU sends a good watchdog refresh before the end of the WDW_RECOVERY duration, the device switches back to the WDW_PERIOD duration and associated duty cycle if the FCCU pins no longer indicate an error. Otherwise, a new WDW_RECOVERY period is started. If the MCU does not send a good watchdog refresh before the end of the WDW_RECOVERY duration, a reset pulse is generated and the Fail-Safe state machine moves back to INIT_FS.

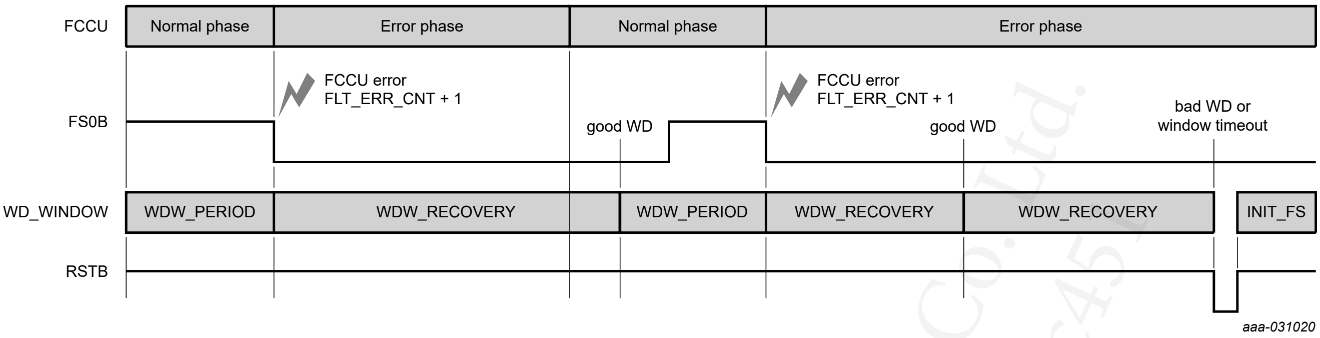


Figure 40. Fault recovery strategy principle

31.5 FCCU monitoring

The FCCU monitoring feature is enabled by the OTP FCCU_EN bit. The FCCU input pins monitor HW failures from the MCU. The FCCU monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh. The FCCU input pins are configured by pair, or single independent inputs with the FCCU_CFG[2:0] bits.

Table 155. FCCU monitoring configuration

FCCU_CFG[2:0]	FCCU pins configuration
000	No monitoring
001 (default)	**FCCU1 and FCCU2 inputs monitoring activated by pair (BI-Stable protocol)**
010	FCCU1 or FCCU2 single input level monitoring activated
011	FCCU1 input level monitoring only, FCCU2 input not used
100	FCCU2 input level monitoring only, FCCU1 input not used
101	FCCU1 or FCCU2 single input PWM monitoring activated
110	FCCU1 input PWM monitoring, FCCU2 input level monitoring
111	FCCU2 input PWM monitoring, FCCU1 input level monitoring
Reset condition	POR

31.5.1 FCCU12 monitoring by pair

When FCCU12 are used by pair, the bi-stable protocol is supported according to figure below:

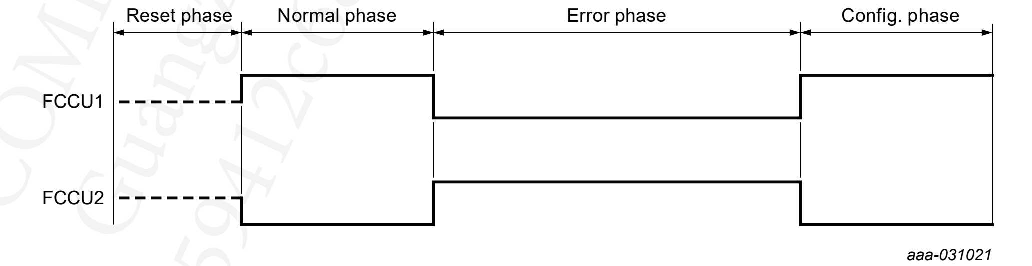


Figure 41. FCCU bi-stable protocol

The polarity of the FCCU fault signals is configurable with FCCU12_FLT_POL bit during the INIT_FS phase.

Table 156. FCCU12 polarity configuration

FCCU12_FLT_POL	FCCU12 polarity
0 (default)	**FCCU1 = 0 or FCCU2 = 1 level is a fault**
1	FCCU1 = 1 or FCCU2 = 0 level is a fault
Reset condition	POR

When an FCCU fault is detected, the Fail-Safe reaction on RSTB and/or FS0B is configurable with the FCCU12_FS_IMPACT bit during the INIT_FS phase.

Table 157. FCCU12 error impact configuration

FCCU12_FS_IMPACT	FCCU12 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

31.5.2 FCCU12 independent monitoring: level and/or PWM

When FCCU1 and/or FCCU2 are used independently, the FCCU inputs can monitor two different and independent error signals. These error signals can be either steady state level signals or PWM signals.

When the error signal(s) is/are steady state level signal(s), the polarity of each FCCU fault signal is configurable with FCCUx_FLT_POL bits during the INIT_FS phase.

Table 158. FCCUx polarity configuration

FCCU1_FLT_POL	FCCU1 polarity
0 (default)	**FCCU1 low level is a fault**
1	FCCU1 high level is a fault
Reset condition	POR
FCCU2_FLT_POL	**FCCU2 polarity**
0 (default)	**FCCU2 low level is a fault**
1	FCCU2 high level is a fault
Reset condition	POR

When the error signal(s) is/are PWM signal(s), the error state is reported when the positive/negative pulse duration in any is < $FCCU12_{HFDET}$ or when the positive/negative pulse duration is > $FCCU12_{LFDET}$

When FCCU fault is detected, the Fail-Safe reaction on RSTB and/or FS0B is configurable with the FCCUx_FS_IMPACT bits during the INIT_FS phase.

Table 159. FCCUx error impact configuration

FCCU1_FS_IMPACT	FCCU1 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**

Table 159. FCCUx error impact configuration*...continued*

FCCU1_FS_IMPACT	FCCU1 impact on RSTB/FS0B
Reset condition	POR
FCCU2_FS_IMPACT	**FCCU2 impact on RSTB/FS0B**
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

31.5.3 FCCU12 electrical characteristics

Table 160. FCCU12 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
FCCU1,2					
$FCCU12_{TERR}$	FCCU1:2 Filter time when PWM monitoring is activated	0.1	—	1.0	µs
	FCCU1:2 Filter time when level monitoring is activated	4.0	6.0	8.0	µs
$FCCU12_{VIH}$	FCCU1,2 High level input voltage	—	—	0.7 x VMON0_I2C	V
$FCCU12_{VIL}$	FCCU1,2 Low level input voltage	0.3 x VMON0_I2C	—	—	V
$FCCU12_{HYST}$	FCCU1,2 input voltage hysteresis	0.1 x VMON0_I2C	—	—	V
$FCCU1_{RPD}$	FCCU1 internal pulldown resistor	400	800	1300	kΩ
$FCCU2_{RPU}$	FCCU2 internal pullup resistor to VMON0_I2C	100	200	400	kΩ
$FCCU12_{RATIO}$	FCCU1/2 internal resistor ratio ($FCCU1_{RPD}$ / $FCCU2_{RPD}$)	3.5	4.0	4.5	—
$FCCU12_{GF}$	FCCU1,2 good frequency range (PWM detection)	10	—	45	kHz
$FCCU12_{BLF}$	FCCU1,2 bad low frequency range (PWM detection)	—	—	5	kHz
$FCCU12_{BHF}$	FCCU1,2 bad high frequency range (PWM detection)	90	—	—	kHz
$FCCU12_{HFDET}$	FCCU1,2 minimum pulse time (both polarities) for PWM HF detection	6.0	8.0	10	µs
$FCCU12_{LFDET}$	FCCU1,2 maximum pulse time (both polarities) for PWM LF detection	51	64	80	µs

31.6 VMON: Voltage Supervisor

The voltage supervisor is in charge of overvoltage and undervoltage monitoring of all VMONx (x = 0 to 9) input pins. When an overvoltage occurs on a FS86 regulator monitored by one of these pins, the associated FS86 regulator (REG_ASSING) is switched off until the fault is removed. The voltage monitoring is active as soon as FS_ENABLE = 1 and UV/OV flags are then reported accordingly. Each VMONx monitoring feature is enabled by OTP.

31.6.1 VMON0_I2C monitoring

The VMON0 input pin can be connected to VPRE, BUCK, LDO1, LDO2 or an external regulator. The regulator connected to VMON0 must be at 1.8 V or 3.3 V to be compatible with overvoltage and undervoltage monitoring thresholds.

31.6.2 VMONx_DAC monitoring (x from 1 to 3)

The three VMONx_DAC input pins can be connected to PF50 or another external regulator. The regulators connected to VMONx_DAC must be between 0.5 V and 1.5 V to be compatible with overvoltage and undervoltage monitoring thresholds.

The VMONx_DAC threshold have 1.0 % UV/OV accuracy at trim target (0.8 V DAC setting, 4.0 % VMON threshold). Threshold UV/OV accuracy varies with DAC and threshold settings not exceeding 1.4 %.

Table 161. DAC voltage monitoring configuration

VMONx_V[7:0]	DAC voltage	VMONx_V[7:0]	DAC voltage
00010000	0.50000 V	00101000	0.80000 V
00010001	0.50625 V	-.-.-.-.-.-.-.-	
00010010	0.51250 V	00110000	0.90000 V
00010011	0.51875 V	-.-.-.-.-.-.-.-	
00010100	0.52500 V	00111000	1.00000 V
00010101	0.53125 V	-.-.-.-.-.-.-.-	
00010110	0.53750 V	01000000	1.10000 V
00010111	0.54375 V	-.-.-.-.-.-.-.-	
00010100	0.55000 V	10000000	1.20000 V
00011001	0.55625 V	-.-.-.-.-.-.-.-	
00011010	0.56250 V	10010000	1.30000 V
00011011	0.56875 V	-.-.-.-.-.-.-.-	
00011100	0.57500 V	10100000	1.40000 V
00011101	0.58125 V	-.-.-.-.-.-.-.-	
00011110	0.58750 V	10101011	1.46875 V
00011111	0.59375 V	10101100	1.47500 V
00011000	0.60000 V	10101101	1.48125 V
-.-.-.-.-.-.-.-		10101110	1.48750 V
00100000	0.70000 V	10101111	1.49375 V
-.-.-.-.-.-.-.-		10110000	1.50000 V

31.6.2.1 Static voltage scaling (SVS)

A static voltage scaling function is implemented on each VMONx_DAC to allow the MCU to reduce the output voltage initially monitored at start-up. The SVS configuration must be done in INIT_FS phase. The offset value is configurable by I2C with the VMONx_SVS[4:0] bits and the exact complemented value must be written in the NOT_VMONx_SVS[4:0] bits.

Table 162. SVS offset configuration

VMONx_SVS[4:0]	NOT_VMONx_SVS[4:0]	Offset applied to VMONx
00000 (default)	**11111**	**0 mV**
00001	11110	-6.25 mV
- - - - -	- - - - -	-6.25 mV step per bit
00010	11101	-12.50 mV
00100	11011	-25.00 mV
01000	10111	-50.00 mV
10000	01111	-100.00 mV

The OV/UV threshold changes immediately when the NOT_VMONx_SVS[4:0] I2C command is received and confirmed good.

To avoid having an undervoltage reaction when reducing the monitored voltage, each VMONx_DAC undervoltage reaction can be masked individually using I2C VMONx_SVS_UV_MASK bit. The undervoltage flag remain active.

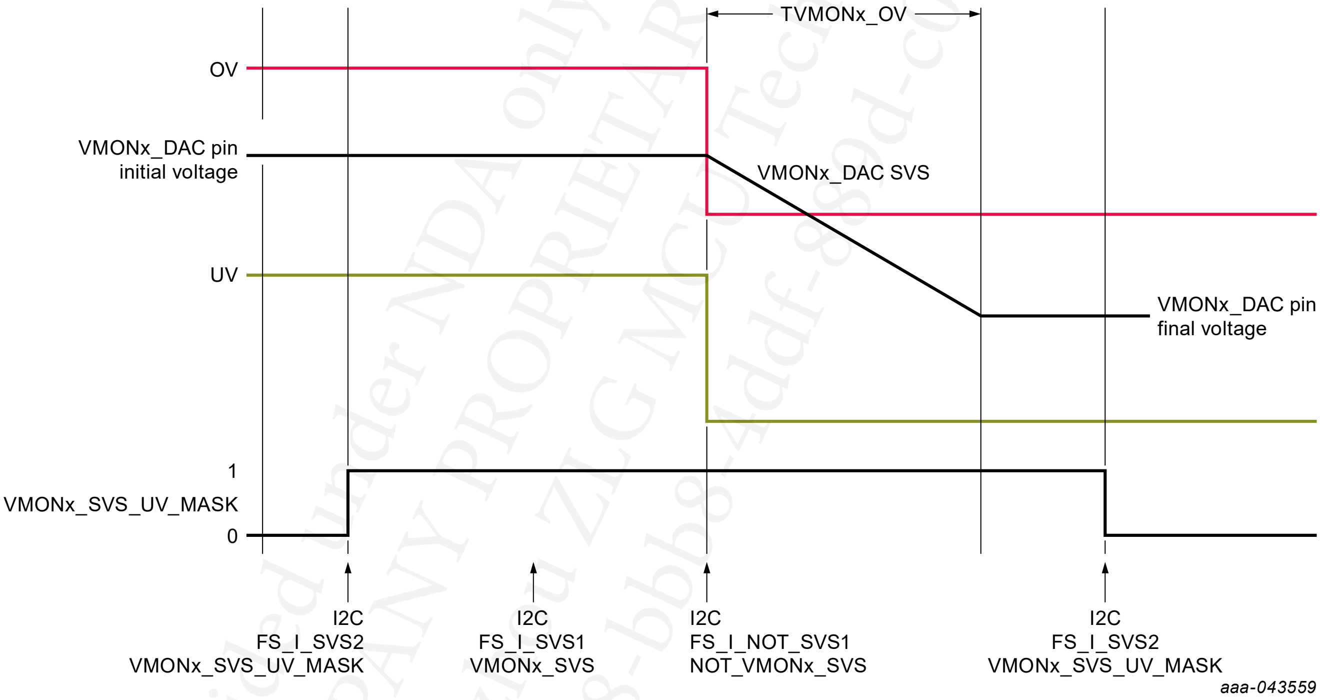


Figure 42. SVS principle time diagram

31.6.3 VMON4_RINT monitoring

VMON4 input pin can be connected to VPRE, BUCK, LDO1, LDO2 or an external regulator. The regulator connected to VMON4 must be at 1.8 V or 3.3 V to be compatible with overvoltage and undervoltage monitoring thresholds.

31.6.4 VMONy_RES monitoring (y from 5 to 9)

The five VMONy_RES input pins can be connected to any FS86 regulators or external regulators. The external resistor bridge connected to VMONy_RES must be calculated to deliver a midpoint of 0.8 V. Use a resistor of ±0.1% accuracy or less.

31.6.5 VMON UV/OV threshold

The OV and UV thresholds are configured independently for each VMONx (x = 0 to 9) by OTP at VMONx_UVTH[1:0] and VMONx_OVTH[1:0].

Table 163. VMON UV/OV thereshold configuration

VMONx_UVTH[3:0] VMONx_OVTH[3:0]	VMONx Undervoltage Threshold configuration	VMONx Overvoltage Threshold configuration
0000	97.5 %	102.5 %
0001	97.0 %	103.0 %
0010	96.5 %	103.5 %
0011	96.0 %	104.0 %
0100	95.5 %	104.5 %
0101	95.0 %	105.0 %
0110	94.5 %	105.5 %
0111	94.0 %	106.0 %
1000	93.5 %	106.5 %
1001	93.0 %	107.0 %
1010	92.5 %	107.5 %
1011	92.0 %	108.0 %
1100	91.5 %	108.5 %
1101	91.0 %	109.0 %
1110	90.5 %	109.5 %
1111	90.0 %	110.0 %

VMON Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Table 164. VMON Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VMON0, VMON4, VMON5 to VMON9, and VMON1 to VMON3 if VMONx_V = 0.8 V					
Undervoltage threshold					

Table 164. VMON Electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
$VMON_{yUVTH}$	OTP VMONy_UVTH = 0000	96.45	97.5	98.55	%
	OTP VMONy_UVTH = 0001	95.97	97	98.03	
	OTP VMONy_UVTH = 0010	95.48	96.5	97.52	
	OTP VMONy_UVTH = 0011	95	96	97	
	OTP VMONy_UVTH = 0100	94.48	95.5	96.52	
	OTP VMONy_UVTH = 0101	93.97	95	96.03	
	OTP VMONy_UVTH = 0110	93.45	94.5	95.55	
	OTP VMONy_UVTH = 0111	92.93	94	95.07	
	OTP VMONy_UVTH = 1000	92.42	93.5	94.58	
	OTP VMONy_UVTH = 1001	91.9	93	94.1	
	OTP VMONy_UVTH = 1010	91.38	92.5	93.62	
	OTP VMONy_UVTH = 1011	90.87	91.5	93.13	
	OTP VMONy_UVTH = 1100	90.35	91	92.65	
	OTP VMONy_UVTH = 1101	89.83	90.5	92.17	
	OTP VMONy_UVTH = 1110	89.32	90	91.68	
	OTP VMONy_UVTH = 1111	88.8	92	91.2	
Overvoltage threshold					
$VMON_{yOVTH}$	OTP VMONy_OVTH = 0000	101.45	102.5	103.55	%
	OTP VMONy_OVTH = 0001	101.97	103	104.03	
	OTP VMONy_OVTH = 0010	102.48	103.5	104.52	
	OTP VMONy_OVTH = 0011	103	104	105	
	OTP VMONy_OVTH = 0100	103.48	104.5	105.52	
	OTP VMONy_OVTH = 0101	103.97	105	106.03	
	OTP VMONy_OVTH = 0110	104.45	105.5	106.55	
	OTP VMONy_OVTH = 0111	104.93	106	107.07	
	OTP VMONy_OVTH = 1000	105.42	106.5	107.58	
	OTP VMONy_OVTH = 1001	105.9	107	108.1	
	OTP VMONy_OVTH = 1010	106.38	107.5	108.62	
	OTP VMONy_OVTH = 1011	106.87	108	109.13	
	OTP VMONy_OVTH = 1100	107.35	108.5	109.65	
	OTP VMONy_OVTH = 1101	107.83	109	110.17	
	OTP VMONy_OVTH = 1110	108.32	109.5	110.68	
	OTP VMONy_OVTH = 1111	108.8	110	111.2	
$VMON0\_I2C_{RPD}$	VMON0_I2C internal passive pull-down	180	430	680	kΩ
$VMON4\_RINT_{RPD}$	VMON4_RINT internal passive pull-down	180	430	680	kΩ
$VMONy\_DAC_{RPD}$	VMONx_DAC internal passive pull-down	1	2	4	MΩ
$VMONx\_RES_{RPD}$	VMONx_RES internal passive pull-down	1	2	4	MΩ

31.6.6 VMON Deglitch Time

To allows the detection of oscillations from the voltage rails connected to any FS86 VMON, an asymmetrical filtering time is used between OV/UV detection (TMON1_UV/OV) and non-detection (TMON2_UV/OV) times. The non-detection time is four times greater than the detection time for any configuration.

The OV and UV deglitch times are configured independently by OTP at VMONx_UV_DGLT[1:0] and VMONx_OV_DGLT[1:0], however some VMON deglitch

times are configured together in the same register, such as VMON04 (VMON 0&4), VMON56 (VMON 5&6), and VMON789 (VMON 7&8&9). These VMON always have the same configuration.

Table 165. VMON deglitch time configuration

VMONx_OV/UV_DGLT[1:0]	OV/UV detection time	OV/UV non-detection time
00	10 µs	40 µs
01	25 µs	100 µs
10	50 µs	200 µs
11	100 µs	400 µs

Note: *Undervoltage and Overvoltage filtering times are set independently.*

Table 166. VMON deglitch time characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VMON04, VMON1, VMON2, VMON3, VMON56 and VMON789					
TMON1_UV/OV	Filtering time to detect an Undervoltage or an Overvoltage				µs
	OTP VMONx_OV/UV_DGLT[1:0] = 00	9.0	10	11	
	OTP VMONx_OV/UV_DGLT[1:0] = 01	22.5	25	27.5	
	OTP VMONx_OV/UV_DGLT[1:0] = 10	45	50	55	
	OTP VMONx_OV/UV_DGLT[1:0] = 11	90	100	110	
TMON2_UV/OV	Filtering time to detect a non-Undervoltage after an undervoltage detection or a non-Overvoltage after an overvoltage detection				µs
	OTP VMONx_OV/UV_DGLT[1:0] = 00	36	40	44	
	OTP VMONx_OV/UV_DGLT[1:0] = 01	90	100	110	
	OTP VMONx_OV/UV_DGLT[1:0] = 10	180	200	220	
	OTP VMONx_OV/UV_DGLT[1:0] = 11	360	400	440	

31.6.7 VMON Safety Reaction (impact)

When an overvoltage or undervoltage fault is detected, the Fail-Safe reaction on RSTB and/or FS0B is configurable with the VMONx_OV/UV_IMPACT[1:0] bits during the INIT_FS phase to each monitoring input.

Note that VMONx_OV/UV_IMPACT[1:0] has no relevance if OTP VMONx_PGOOD = 1 because PGOOD assertion causes FS0B and RSTB assertion.

Table 167. VMONx safety reaction (impact) configuration (x from 0 to 9)

VMONx_OV_FS_IMPACT[1:0]	NOT_VMONx_OV_FS_IMPACT[1:0]	VMONx OV impact on RSTB/FS0B
00	11	No effect on RSTB and FS0B
01	10	FS0B only is asserted
10	01	FS0B and RSTB are asserted
11 (default)	**00 (default)**	**FS0B and RSTB are asserted**
VMONx_UV_FS_IMPACT[1:0]	**NOT_VMONx_UV_FS_IMPACT[1:0]**	**VMONx UV impact on RSTB/FS0B**

Table 167. VMONx safety reaction (impact) configuration (x from 0 to 9)...continued

VMONx_OV_FS_IMPACT[1:0]	NOT_VMONx_OV_FS_IMPACT[1:0]	VMONx OV impact on RSTB/FS0B
00	11	No effect on RSTB and FS0B
01 (default)	**10 (default)**	**FS0B only is asserted**
10	01	FS0B and RSTB are asserted
11	00	FS0B and RSTB are asserted

31.6.8 VMON regulator assignment

In order to turn off the regulator when an overvoltage detection occurs, the VMON can be assigned with a specific regulator using VMON0_REG_ASSIGN[2:0] by I2C and, in some cases, also by OTP. If an external regulator is connected to a VMON, this regulator cannot be turned off, but the over- voltage flag is reported to the MCU, which can take appropriate action.

Table 168. VMON regulator assignment OTP/I2C configurability (Main)

VMONx regulator assignment	OTP	I2C
VMON0_REG_ASSIGN	YES (POR value)	YES
VMON1_REG_ASSIGN	YES (POR value)	YES
VMON2_REG_ASSIGN	NO	YES
VMON3_REG_ASSIGN	NO	YES
VMON4_REG_ASSIGN	YES (POR value)	YES
VMON5_REG_ASSIGN	NO	YES
VMON6_REG_ASSIGN	NO	YES
VMON7_REG_ASSIGN	NO	YES
VMON8_REG_ASSIGN	NO	YES
VMON9_REG_ASSIGN	NO	YES

Table 169. VMONx regulator assignment configuration (x from 0 to 9)

VMONx_REG_ASSIGN[2:0] (OTP) VMONx_REG[2:0] (I2C)	VMONx assigned to
000 (default)	**External Regulator (flag only if OV)**
001	VPRE (shutdown if OV)
010	LDO1 (shutdown if OV)
011	LDO2 (shutdown if OV)
100	BOOST (shutdown if OV)
101	BUCK (shutdown if OV)
110	PWRDWN_DFS (DEEP-FS if OV)
111	External Regulator (flag only if OV)

31.6.9 Electrical characteristics

Table 170. VMON_DAC Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VMONx_DAC (x from 1 to 3)					
DAC_min	Voltage monitoring threshold minimum	—	0.5	—	V
DAC_max	Voltage monitoring threshold maximum	—	1.5	—	V
DAC_step	Voltage monitoring threshold steps (OTP configurable)	—	6.25	—	mV
DAC_acc_target	DAC accuracy at OTP VMONx_V = 0.8 V	−1.0	—	1.0	%
DAC_acc_dev_max	Additional DAC accuracy deviation at DAC_max = 1.5 V and DAC_min = 0.5 V	−0.2	—	0.2	%
DAC_acc_dev_pos	DAC accuracy deviation at any DAC setting between 0.8 V and 1.5 V DAC_acc_dev = abs((OTP VMONx_V − DAC_acc_target) * DAC_acc_dev_max) / abs(OTP VMONx_V_max − DAC_acc_target)	–DAC_acc_dev_pos	—	DAC_acc_dev_pos	%
DAC_acc_dev_neg	DAC accuracy deviation at any DAC setting between 0.8 V and 0.5 V DAC_acc_dev = abs((OTP VMONx_V − DAC_acc_target) * DAC_acc_dev_min) / abs(OTP VMONx_V_max − DAC_acc_target)	–DAC_acc_dev_neg	—	DAC_acc_dev_neg	%
VMONx_min	Undervoltage and Overvoltage threshold minimum	—	+2.5	—	%
VMONx_max	Undervoltage and Overvoltage threshold maximum	—	+10	—	%
VMONx_step	Undervoltage and Overvoltage threshold step	—	+0.5	—	%
VMONx_acc_target	VMONx accuracy at trim target, *valid for OTP VMONx_V = 0.8 V and OTP VMONx_TH = 4%*	−1.0	—	1.0	%
VMONx_acc_dev_max	Additional VMONx accuracy deviation at VMONx_max = 10%, *valid for OTP VMONx_V = 0.8 V*	−0.2	—	0.2	%
VMONx_acc_dev	VMONx accuracy deviation at any UVOV threshold, valid for OTP VMONx_V = 0.8 V VMONx_acc_dev = abs((OTP VMONx_TH − VMONx_acc_target) * VMONx_acc_dev_max) / abs(OTP VMONx_TH_max − VMONx_acc_target)	VMONx_acc_dev	—	VMONx_acc_dev	%
VMONx_acc_tot_pos	VMONx total accuracy at any UVOV threshold, valid for any OTP VMONx_V setting VMONx_acc_tot = VMONx_acc_target + VMONx_acc_dev + DAC_acc_dev_pos	VMONx_acc_tot_pos	—	VMONx_acc_tot_pos	%
VMONx_acc_tot_neg	VMONx total accuracy at any UVOV threshold, valid for any OTP VMONx_V setting VMONx_acc_tot = VMONx_acc_target + VMONx_acc_dev + DAC_acc_dev_neg	VMONx_acc_tot_neg	—	VMONx_acc_tot_neg	%

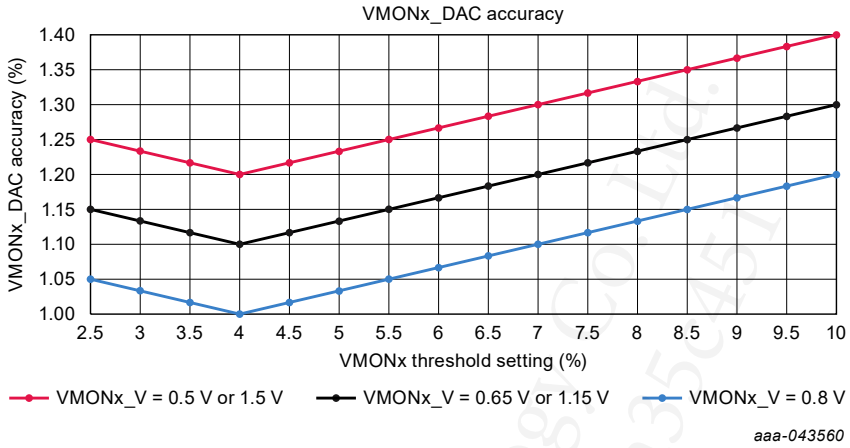


Figure 43. VMONx_DAC accuracy plot

Notes:

- *VMON0_I2C, VMON4_RINT, VMONy_RES (y = 5 to 9) have the same accuracy as VMONy_DAC with VMONx_V = 0.8 V (x = 1 to 3).*
- *The x axis corresponds to the UV/OV threshold computed as (100 ±x) %, with (–) for UV and (+) for OV. The y value represents the threshold tolerance, being (100 ±x)% ±y%. For example, in the case VMONx_V = 0.8 V and VMONx OV threshold setting equals to 4% (x = 4.0%, y = 1.0%), the threshold is (104.0 ±1.0) %.*

31.7 ERRMON: External IC monitoring

The external IC monitoring feature is enabled by OTP ERRMON_EN bit. The ERRMON input pin is in charge of monitoring an external IC that is not the FS86 or the MCU. The ERRMON monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh. When an error is identified, the MC has a maximum "acknowledge time" to clear the error in the I2C ERRMON_ACK bit before the configured safety reaction is triggered.

A transition detected at the ERRMON pin indicates an error from the external IC. The polarity of the ERRMON fault signal is configurable with ERRMON_FLT_POL bit during the INIT_FS phase.

Table 171. ERRMON polarity configuration

ERRMON_FLT_POL	ERRMON polarity
0 (default)	**Negative edge at ERRMON pin is a fault**
1	Positive edge at ERRMON pin is a fault
Reset condition	POR

The acknowledge timing from the MCU is configurable with the ERRMON_ACK_TIME[1:0] bits. When this timing is set to 0 ms, the ERRMON pin can be used as an additional FCCU pin with immediate reaction on RSTB/FS0B depending on ERRMON_FS_IMPACT configuration.

Table 172. ERRMON acknowledgement time configuration

ERRMON_ACK_TIME[1:0]	ERRMON acknowledgement timing
00	1 ms

Table 172. ERRMON acknowledgement time configuration*...continued*

ERRMON_ACK_TIME[1:0]	ERRMON acknowledgement timing
01 (default)	**8 ms**
10	32 ms
11	0 ms
Reset condition	POR

The acknowledgement by the MCU is done through I2C communication according to the figure below:

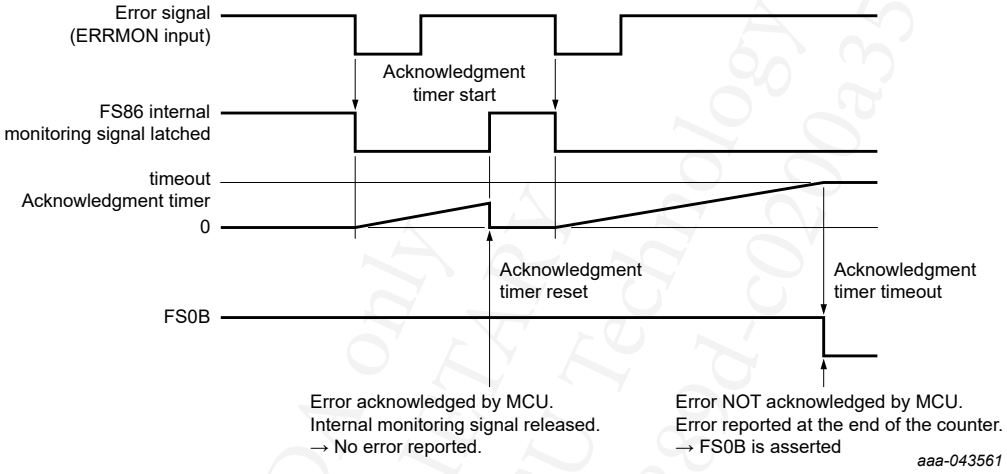


Figure 44. ERRMON timing diagram

When an ERRMON fault is detected, the Fail-Safe reaction on RSTB and/or FS0B is configurable with the ERRMON_FS_IMPACT bit during the INIT_FS phase.

Table 173. ERRMON Fail-safe impact

ERRMON_FS_IMPACT	ERRMON impact on RSTB/FS0B
0	FS0B only is asserted when ERRMON fault is detected
1 (default)	**FS0B and RSTB are asserted when ERRMON fault is detected**
Reset condition	POR

31.7.1 Electrical characteristics

Table 174. ERRMON electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
ERRMON					
$ERRMON_{ACC\_TIME}$	Acknowledgement time				ms
	ERRMON_ACK_TIME[1:0] = 00	0.9	1.0	1.1	
	ERRMON_ACK_TIME[1:0] = 01	7.2	8.0	8.8	
	ERRMON_ACK_TIME[1:0] = 10	28.8	32	35.2	
	ERRMON_ACK_TIME[1:0] = 11	—	0	—	

Table 174. ERRMON electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$ERRMON_{TERR}$	Filtering time	4.0	—	8.0	us
$ERRMON_{VIH}$	High level input voltage	—	—	1.5	V
$ERRMON_{VIL}$	Low level input voltage	0.7	—	—	V
$ERRMON_{HYST}$	Input voltage hysteresis	100	—	—	mV
$ERRMON_{IPD}$	Internal pulldown	200	400	800	kΩ

31.8 Fault Management

31.8.1 Fault Error Counter

The FS86 integrates a configurable Fault Error Counter which counts the number of faults related to the device itself and also faults caused by external events. The Fault Error Counter starts at one after a POR or after resuming from Standby. The final value of the Fault Error Counter is used to transition into DEEP-FS mode. The maximum value of this counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bits during the INIT_FS phase.

Table 175. Fault Error Counter configuration

FLT_ERR_CNT_LIMIT[1:0]	Fault Error Counter max value configuration	Fault Error Counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6
Reset condition	POR	

The Fault Error Counter has two output values: intermediate and final. The intermediate value can be used to force the FS0B activation or generate a RSTB pulse according to the FLT_ERR_IMPACT[1:0] bits configuration.

Table 176. Fault Error Counter Fail-Safe impact

FLT_ERR_IMPACT[1:0]	Fault Error Counter intermediate value impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted if FLT_ERR_CNT = intermediate value
10 (default)	**FS0B is asserted if FLT_ERR_CNT = intermediate value** **RSTB pulse is generated when FLT_ERR_CNT = intermediate value**
11	FS0B is asserted if FLT_ERR_CNT = intermediate value RSTB pulse is generated when FLT_ERR_CNT = intermediate value
Reset condition	POR

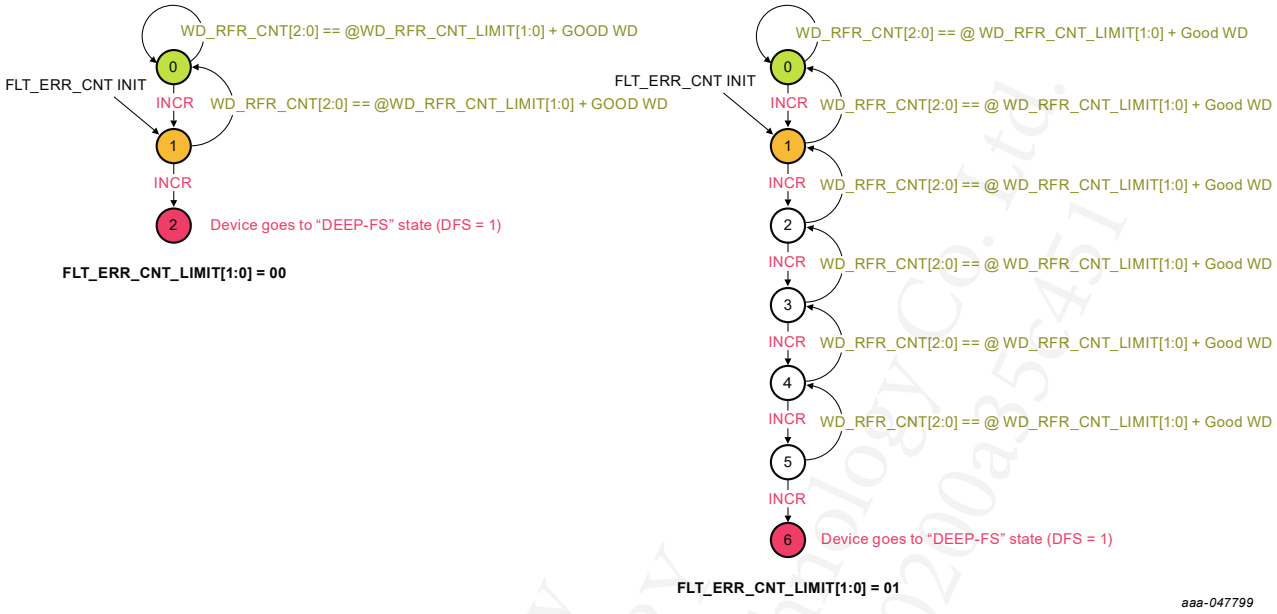


Figure 45. Fault Error Counter diagram with maximum value = 2 or 6

Figure 46. Fault Error Counter diagram with maximum value = 8 or 12

31.8.2 Fault source and reaction

In normal operation when FS0B and RSTB are released, the Fault Error Counter is incremented when a Fault is detected by the FS86 Fail-Safe State Machine. Table 177 lists all the faults and their impact on PGOOD, RSTB and FS0B pins according to the device configuration. The faults that are configured to not assert RSTB and FS0B will not increment the fault error counter. In that case, only the flags are available for MCU diagnostics. The fault error counter is incremented by one each time the FS0B/ RSTB is driven low by the device and when RSTB is asserted low externally. The fault error counter is not incremented when FS0B is asserted low externally. When FS0B is asserted, the Fault Error Counter continues to be incremented by one each time the WD Error Counter reaches its maximum value.

Table 177. Application related fail-safe fault list and reaction

Orange cells = the reaction is not configurable

Green cells = the reaction is configurable by OTP for PGOOD and by I2C for RSTB/FS0B during INIT_FS

Apps related fail-safe faults	FLT_ERR_CNT[3:0]	FS0B assertion	RSTB assertion	PGOOD assertion
VMONx_OV	+1[1]	VMONx_OV_IMPACT[0]	VMONx_OV_IMPACT[1]	VMONx_PGOOD
VMONx_UV	+1[1]	VMONx_UV_IMPACT[0]	VMONx_UV_IMPACT[1]	VMONx_PGOOD
FCCU12 (pair)	+1	Yes	FCCU12_IMPACT	No
FCCU1 (single)	+1	Yes	FCCU1_IMPACT	No
FCCU2 (single)	+1	Yes	FCCU2_IMPACT	No
ERRMON	+1	Yes	ERRMON_IMPACT	No
WD_ERR_CNT[3:0] overflow	+1[1]	WD_FS_IMPACT[0]	WD_FS_IMPACT[1]	No
Fault error counter impact at intermediate Value	—	FAULT_ERR_IMPACT[0]	FAULT_ERR_IMPACT[1]	No
Wrong WD refresh in INIT_FS	+1	Yes	Yes	No
No WD refresh in INIT_FS	+1	Yes	Yes	No
External RESET (out of extended RSTB)	+1	No[2]	Yes (low externally)	No
RSTB pulse request by MCU	—	No[2]	Yes	No
RSTB short to high	+1	Yes	No (high externally)	No
FS0B short to high	—	No (high externally)	FS0B_SC_HIGH_CFG	No
FS0B request by the MCU	—	Yes	No	No
REG_CORRUPT = 1	+1	Yes	No	No
OTP_CORRUPT = 1	+1	Yes	No	No
GO_TO_INITFS request by MCU	—	Yes	No	No

[1] Fault error counter FLT_ERR_CNT[3:0] incremented only if FS0B is asserted. Note that FS0B can be asserted as cascaded effect from RSTB or PGOOD assertion.

[2] By cascaded effect, the FS0B is asserted low in INIT_FS state

- If OTP RSTB2PGOOD = ‘0’ (default configuration), the RSTB and PGOOD pins work independently according to the above table.
- If OTP RSTB2PGOOD = ‘1’, RSTB and PGOOD pins work concurrently and all the faults asserting RSTB will also assert PGOOD, except when an external RESET is detected.

31.8.3 DEEP-FS mode

FS86 enters in Deep Fail-safe (DEEP-FS) mode when:

- The Fault Error Counter reaches its maximum value (not configurable);
- RSTB is asserted low for 8 s (if RSTB monitoring not disabled by OTP RSTB_8S_DIS);
- XFAILB pin is not released before $XFAILB_{TIMEOUT}$ during power-up sequence (if XFAILB synchronization enabled by OTP);
- When the first fault is detected (if configured by I2C during INIT_FS).
- When VPRE voltage > VPRE_FB_OV;
- When VPRE_SW voltage > VPRE_SW_OV before VPRE enable if BAT_SW function is used.

31.9 PGOOD, RSTB, FS0B

The following safety output pins have a hierarchical implementation in order to guarantee the safe state:

- PGOOD has priority 1. If PGOOD is asserted, RSTB and FS0B are asserted.
- RSTB has priority 2. If RSTB is internally asserted, FS0B is asserted but PGOOD may not be asserted.
- FS0B has priority 3. If FS0B is asserted, RSTB and PGOOD may not be asserted.

RSTB release is managed by the Fail-Safe state machine and depends on PGOOD release and ABIST1 execution. Voltage monitoring assigned to PGOOD and to ABIST1 determines when RSTB is released. This configuration is done by OTP.

31.9.1 PGOOD

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU. PGOOD requires an external pull-up resistor to VMON0_I2C and a filtering capacitor to GND for immunity. An internal pull-down resistor (RPD) ensures that PGOOD remains low in Power-Down mode. All VMONx can be assigned to PGOOD by OTP individually using VMONx_PGOOD (x = 0 to 9). PGOOD is asserted low by the FS_LOGIC when any of the assigned regulators are in undervoltage or overvoltage. When PGOOD is asserted low, RSTB and FS0B are also asserted low. An internal pull-up on the gate of the low side MOS ensures PGOOD remains low when an FS_LOGIC failure occurs.

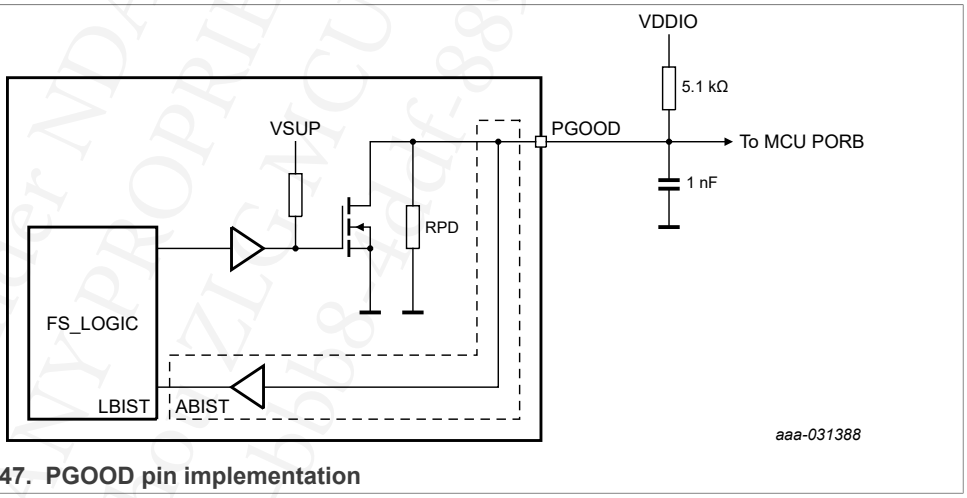


Figure 47. PGOOD pin implementation

Table 178. PGOOD electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
PGOOD					
$PGOOD_{VIL}$	Low level input voltage	0.7	—	—	V
$PGOOD_{VIH}$	High level input voltage	—	—	1.5	V
$PGOOD_{HYST}$	Input voltage Hysteresis	100	—	—	mV
$PGOOD_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.5	V

Table 178. PGOOD electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$PGOOD_{RPD}$	Internal pulldown resistor	200	400	800	kΩ
$PGOOD_{ILIM}$	Current limitation	4.0	—	20	mA
$PGOOD_{TFB}$	Feedback filtering time	8.0	—	15	µs

31.9.2 RSTB

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU. RSTB requires an external pull-up resistor to VMON0_I2C and a filtering capacitor to GND for immunity. An internal pull-down resistor (RPD) ensures RSTB low level in Power-Down mode. RSTB assertion depends on the device configuration during INIT_FS phase. When RSTB is asserted low, FS0B is also asserted low. An internal pull-up on the gate of the low side MOS ensures RSTB remains low when an FS_LOGIC failure occurs. When RSTB is stuck low for more than $RSTB_{T8S}$, the device transition into DEEP-FS mode. This reaction can be disabled using the FS_I_FSSM init register DIS_8S bit and the FS_NOT_I_FSSM init register NOT_DIS_8S.

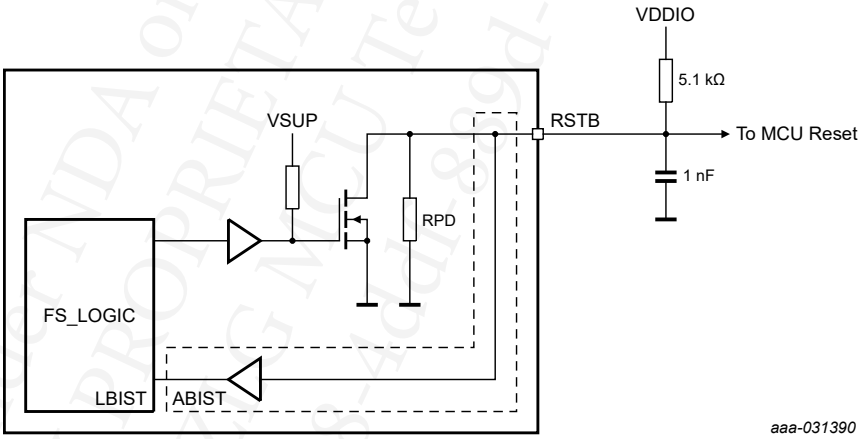


Figure 48. RSTB pin implementation

A 10 ms delay can be added using OTP RSTB_DLY bit when ABIST1 is started and before RSTB is released to accommodate specific MCU requirement asking for voltage supply stabilization before RSTB is released.

Table 179. RSTB electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
RSTB					
$RSTB_{VIL}$	Low level Input voltage	0.7	—	—	V
$RSTB_{VIH}$	High level Input voltage	—	—	1.5	V
$RSTB_{HYST}$	Input voltage hysteresis	100	—	—	mV
$RSTB_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.5	V

Table 179. RSTB electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$RSTB_{RPB}$	Internal pull-down resistor	200	400	800	kΩ
$RSTB_{ILIM}$	Current limitation	4.0	—	20	mA
$RSTB_{TFB}$	Feedback filtering time	8.0	—	15	µs
$RSTB_{TSC}$	Short to high filtering time	500	—	800	µs
$RSTB_{DUR}$	Reset pulse duration				
	RSTB_DUR = 0	9.0	10	11	ms
	RSTB_DUR = 1	0.9	1.0	1.1	
$RSTB_{T8S}$	8 second timer duration	7.0	8.0	9.0	s

31.9.3 FS0B

FS0B is an open-drain output that can be used to transition the system into Safe State. FS0B requires an external pull-up resistor to VMON0_I2C or VSUP, a 10 nF filtering capacitor to GND for immunity when FS0B is a local pin and an additional RC network when FS0B is a global pin to be robust against ESD GUN and ISO 7637 transient pulses. An internal pull-down resistor (RPD) ensures FS0B remains low in Power-Down mode. FS0B assertion depends on the device configuration during INIT_FS phase. An internal pull-up on the gate of the low side MOS ensure FS0B remains low when an FS_LOGIC failure occurs.

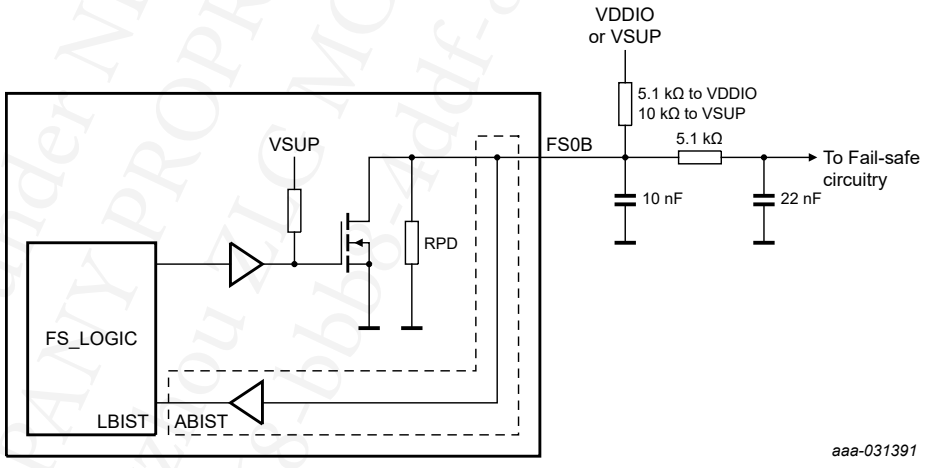


Figure 49. FS0B pin implementation

Table 180. FS0B electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
FS0B					
$FS0B_{VIL}$	Low level Input voltage	0.7	—	—	V
$FS0B_{VIH}$	High level Input voltage	—	—	1.5	V

Table 180. FS0B electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$FS0B_{HYST}$	Input voltage hysteresis	100	—	—	mV
$FS0B_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.5	V
$FS0B_{RPD}$	Internal pull-down resistor	1	2	4	MΩ
$FS0B_{ILIM}$	Current limitation	4.0	—	22	mA
$FS0B_{TFB}$	Feedback filtering time	8.0	—	15	µs
$FS0B_{TSC}$	Short to high filtering time	500	—	800	µs

31.9.4 FS0B release

When the Fail-Safe output FS0B is asserted low by the device due to a fault, some conditions must be validated before allowing the pin to be released by the device. These conditions are:

- LBIST_OK = ABIST1_OK = ABIST2_OK = 1;
- Fault Error Counter = 0;
- RELEASE_FS0B register filled with ongoing WD_SEED reversed and complemented.

Table 181. FS0B release

RELEASE_FS0B[15:8]	B15	B14	B13	B12	B11	B10	B9	B8
WD_SEED	Not(B0)	Not(B1)	Not(B2)	Not(B3)	Not(B4)	Not(B5)	Not(B6)	Not(B7)
RELEASE_FS0B[7:0]	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
WD_SEED	Not(B8)	Not(B9)	Not(B10)	Not(B11)	Not(B12)	Not(B13)	Not(B14)	Not(B15)

31.10 Built in Self-Test (BIST)

31.10.1 Logical BIST

The Fail-safe State Machine includes a Logical Built in Self-Test (LBIST) to verify the correct functionality of the safety logic monitoring. The LBIST is performed after each POR or after each wake up from Standby. In case of an LBIST fail, RSTB and PGOOD are released but FS0B remains stuck low and cannot be released. The flag LBIST_OK is available through I2C for MCU diagnostics. The typical LBIST duration is 4.2 ms and the maximum LBIST duration is 6.0 ms.

31.10.2 Analog BIST

The Fail-Safe State Machine includes two Analog Built in Self-Test (ABIST) to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR, or after each wake up from Standby. The assignment of which regulator is checked during ABIST1 is done by OTP.

ABIST2 is executed after INIT_FS is closed with a good WD refresh and the regulators assigned to ABIST2 during INIT_FS are started and have crossed their UV threshold. In case of an ABIST1 fails, RSTB and PGOOD are released but FS0B remains stuck low

and cannot be released. The flags ABIST1_OK and ABIST2_OK are available thru I2C for MCU diagnostics.

Table 182. ABIST1 coverage

Parameter	Over voltage	Under voltage	Short to High	ABIST1	ABIST2
VMON0 to VMON9	X	X		OTP	I2C
V1p6D_FS	X			X	
PGOOD			X	X	
RSTB			X	X	
FS0B			X	X	

The ABIST2 coverage is configured by I2C in the Fail-Safe registers FS_I_VMON_ABIST2 and its complement FS_I_NOT_VMON_ABIST2.

Table 183. ABIST2 execution bit

VMONx_ABIST2	NOT_VMONx_ABIST2	VMONx BIST executed during ABIST2
0 (default)	**1**	**No ABIST2**
1	0	VMONx ABIST executed during ABIST2
Reset condition		POR

Table 184. ABIST electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
ABIST					
$ABIST1_{TDUR}$	ABIST1 duration MIN with no voltage monitoring assigned by OTP MAX with all voltage monitoring assigned by OTP	125	—	350	µs
$ABIST2_{TDUR}$	ABIST2 duration MIN with no voltage monitoring selected by I2C MAX with all voltage monitoring selected by I2C	125	—	350	µs

31.11 Cyclic CRC check

To guarantee the integrity of mirror registers containing the fuse information (loaded at power-up sequence), a CRC check is launched automatically each 5 ms (T_{CRC}) (<FTTI). The OTP controller (Fail-Safe side) recalculates the CRC for all sectors. If a mismatch is reported, the OTP_CORRUPT bit is set and the Fail-Safe output (FS0b) is asserted.

Table 185. Cyclic CRC check characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = V_{SUP_UVH} to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Cyclic CRC check					
T_{CRC}	CRC check timing interval	4.0	5.0	6.0	ms

32 Application information

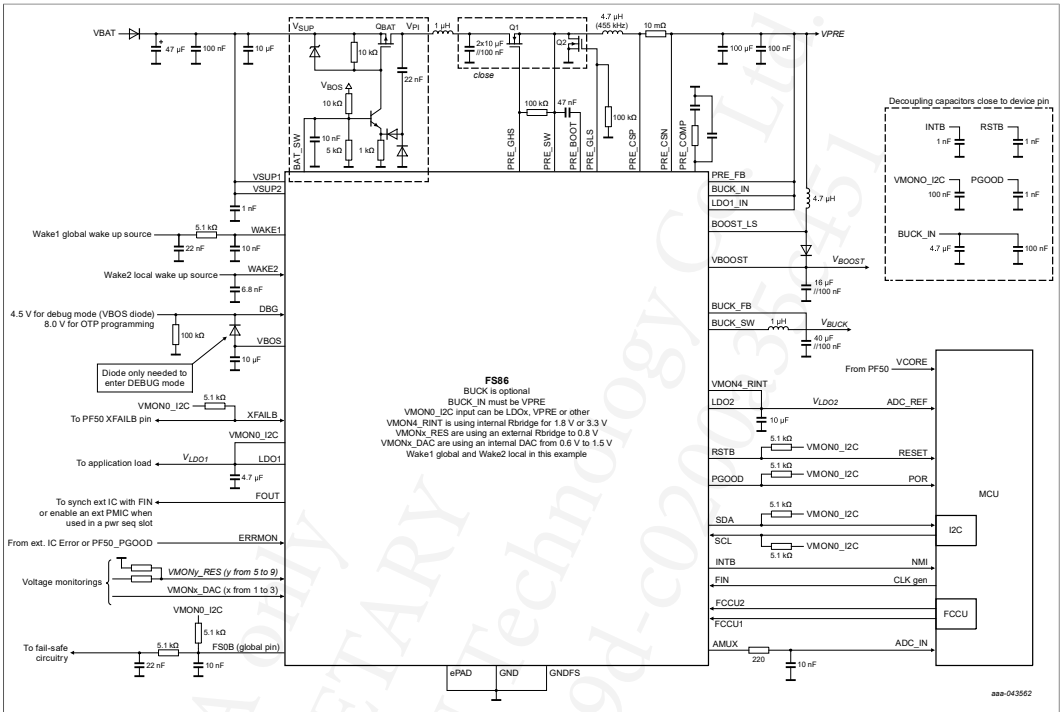


Figure 50. Application schematic

33 Package drawing

FS86 package is a QFN, thermally enhanced, wettable flanks, 7 x 7 x 0.85 mm, 0.5 mm pitch, 48 pins.

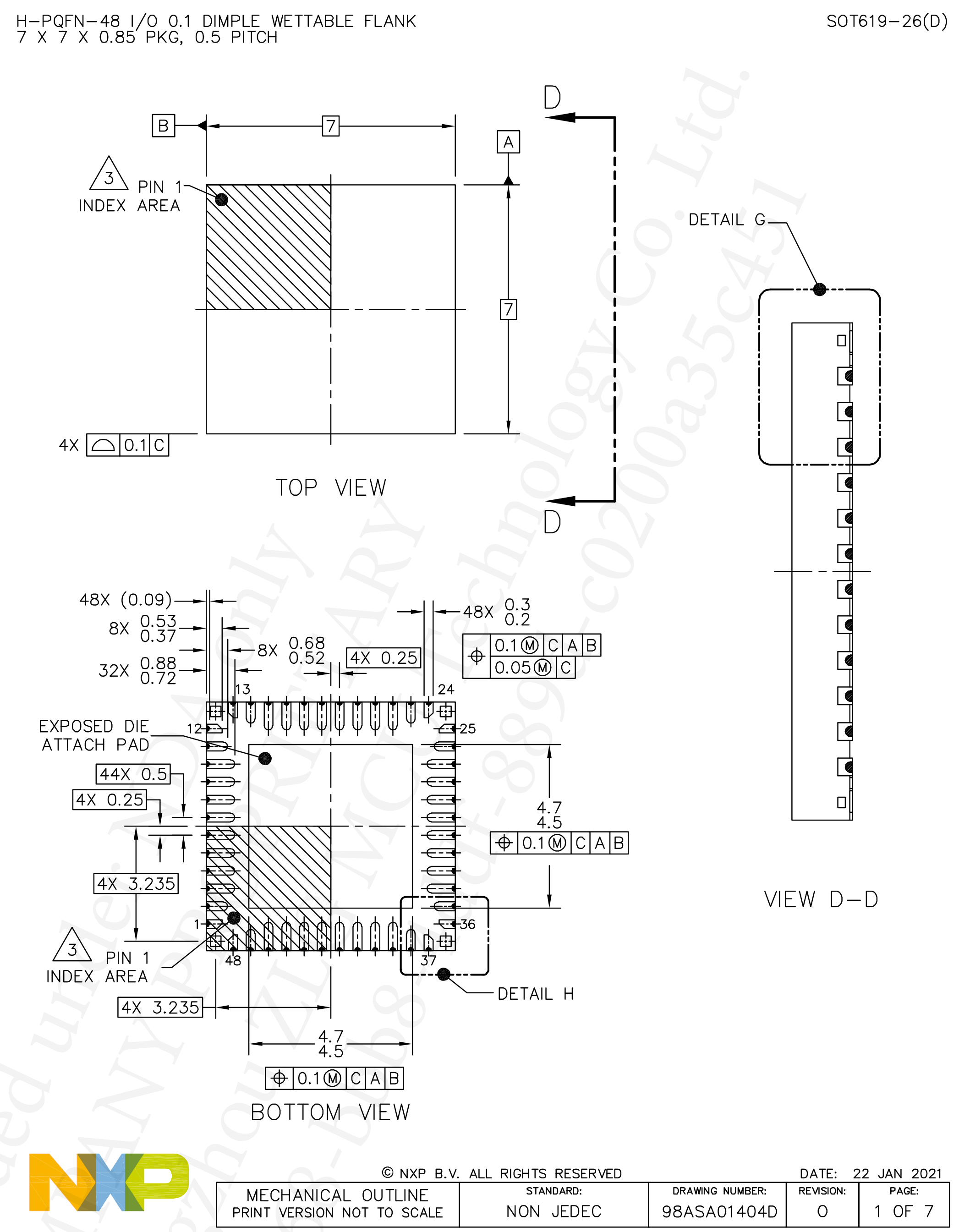


Figure 51. Package drawing − top and bottom view

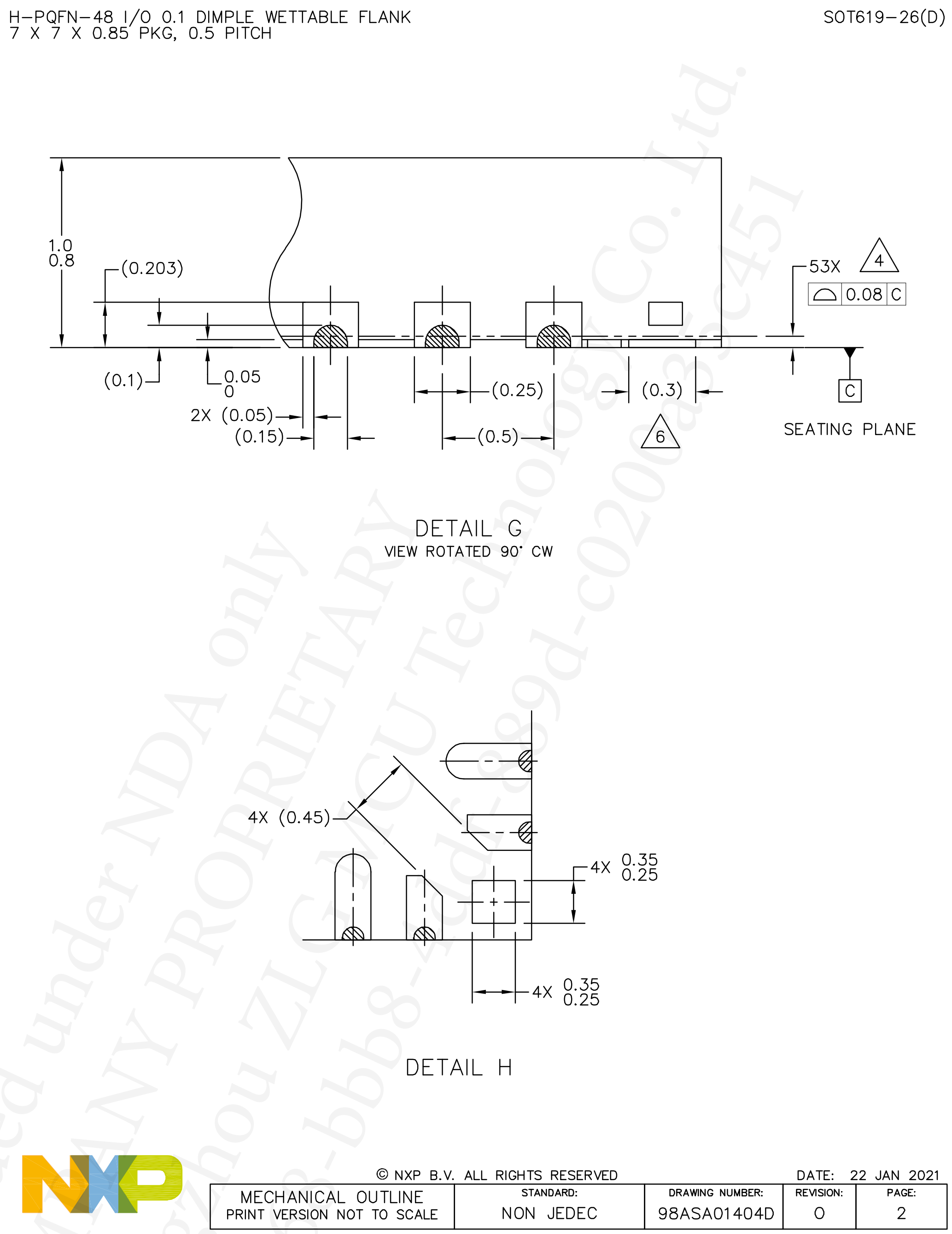


Figure 52. Package drawing − dimple wettable flank

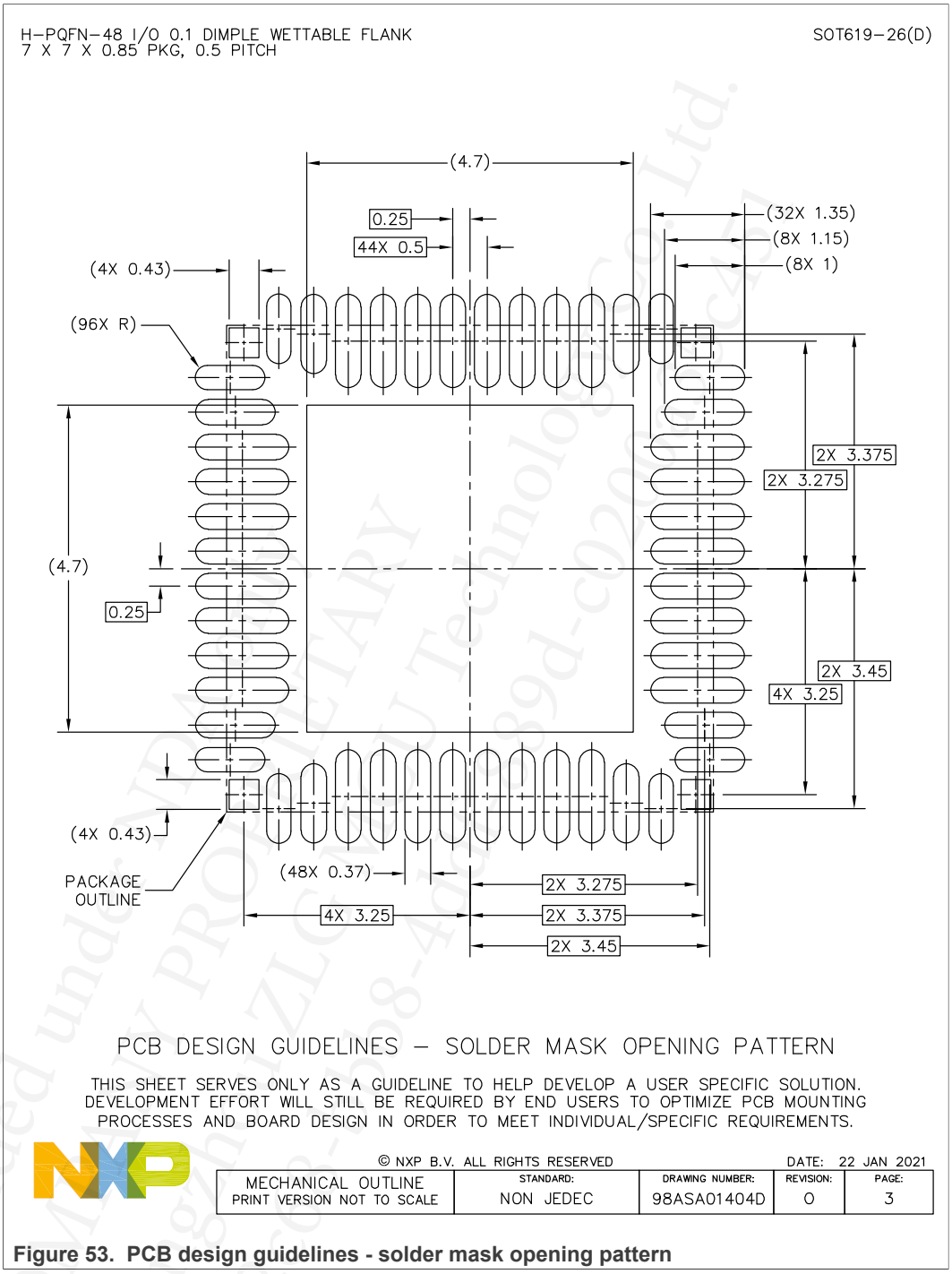


Figure 53. PCB design guidelines - solder mask opening pattern

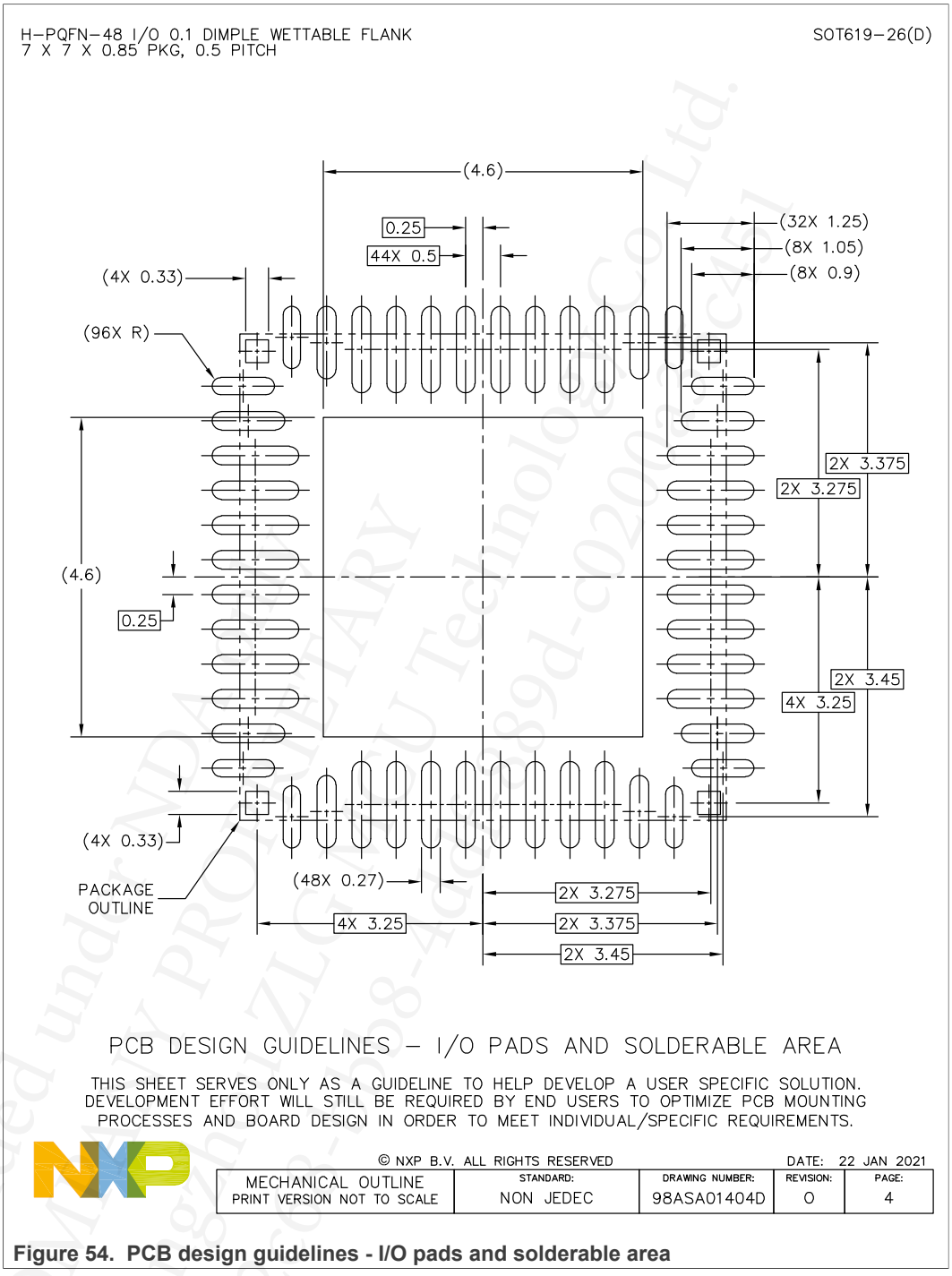
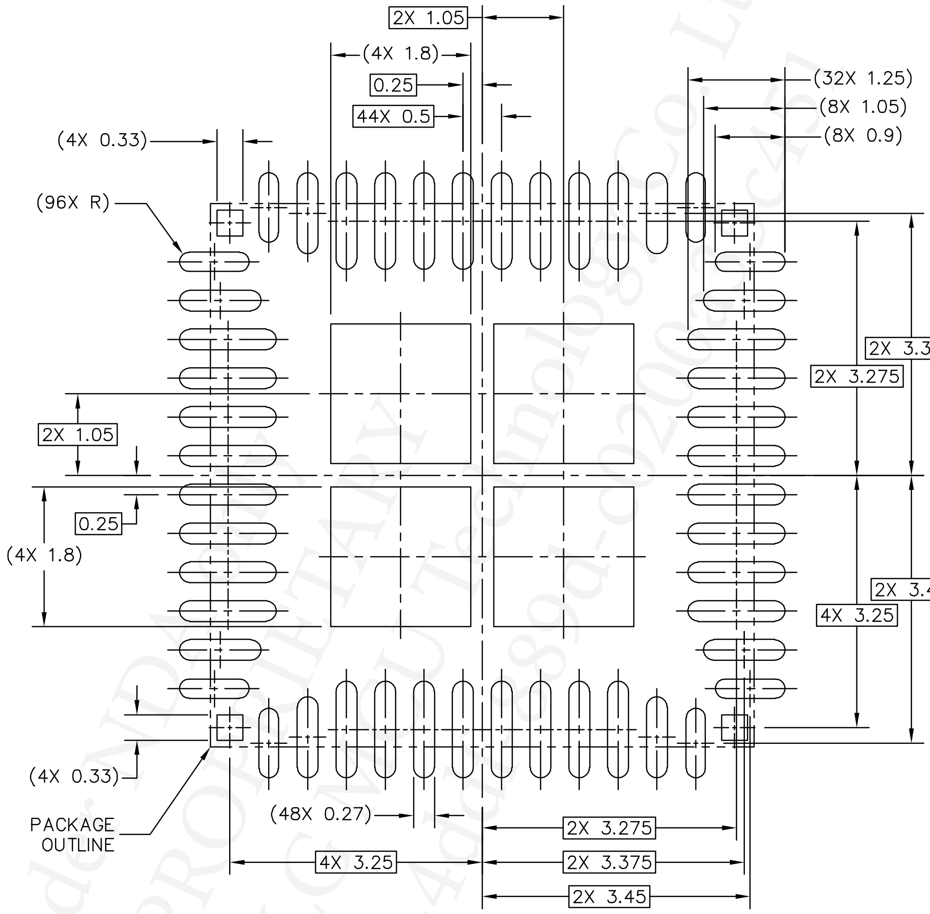


Figure 54. PCB design guidelines - I/O pads and solderable area

H-PQFN-48 I/O 0.1 DIMPLE WETTABLE FLANK
7 X 7 X 0.85 PKG, 0.5 PITCH

SOT619-26(D)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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	NON JEDEC	98ASA01404D	O	5

Figure 55. PCB design guidelines - solder paste stencil

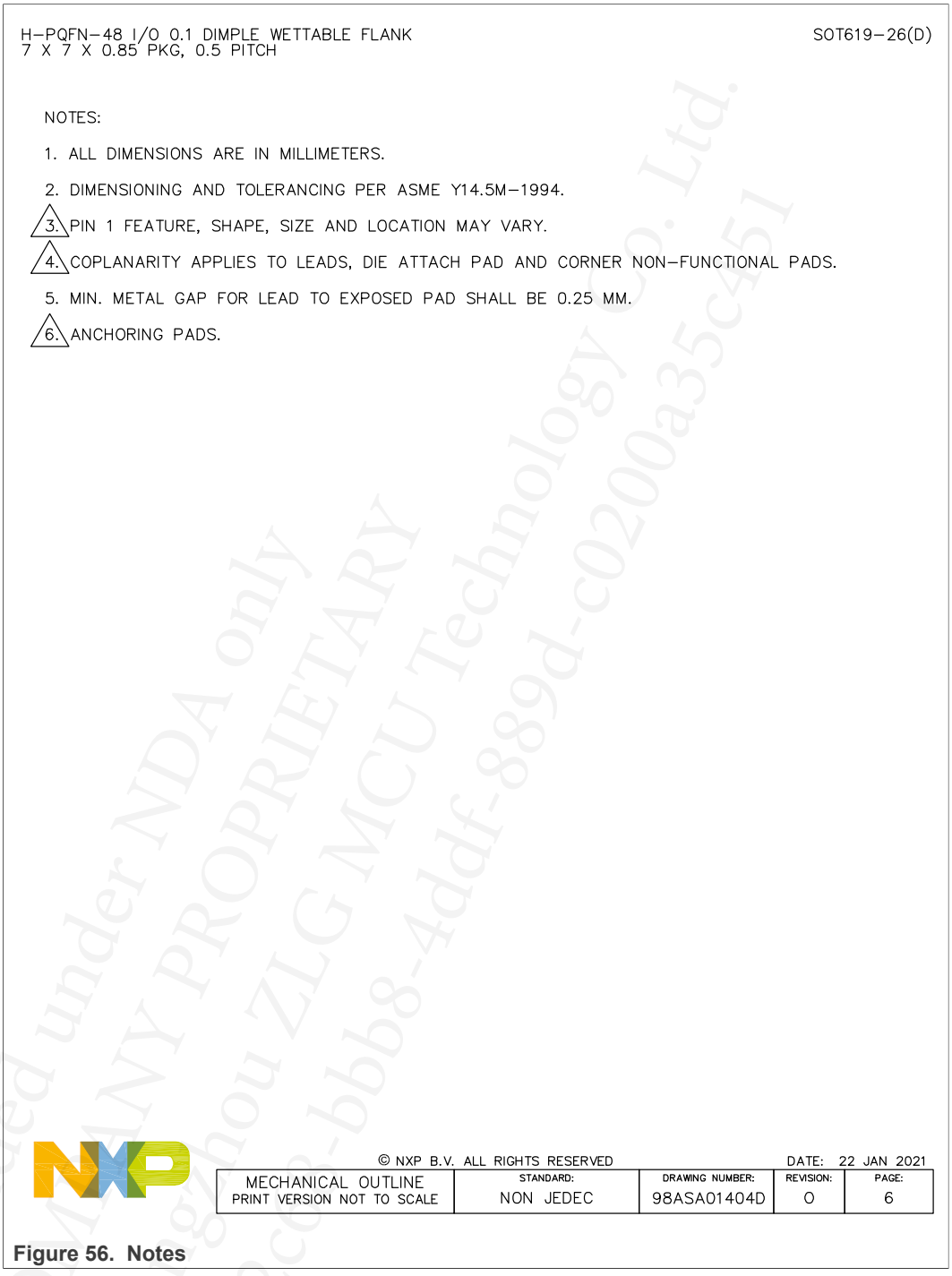

Figure 56. Notes

34 Revision History

Table 186. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FS8600 v. 2	20221202	Product	202212001I	FS8600 v.1
Modifications:	• Updated Section 1. • Updated Section 2. • Updated Figure 1. • In Section 6, updated Figure 2. • Updated footnotes in Section 5.1, Table 1. • In Section 11, updated Figure 4, and Figure 5, and added legend for figures and note. • Under Section 14 updated Figure 6. • In Section 13, Table 7, added $I_{SUP\_STANDBY}$ and V_{SUP} values for 24 V and 12 V power supplies • Updated Section 14.2. • In Section 14.4, updated Figure 7 and Figure 8. • In Section 14.4, added description to Table 9. • In Section 14.6, updated Figure 10. • Clarified mode names in Section 14.7 • In Section 14.5, updated Figure 9 • In Section 17, in the Table 16, corrected field names for registers M_VMON1_REGX and M_VMON2_REGX. • Corrected links and field names in Section 17.14, Table 41. • Corrected links and field names in Section 17.15, Table 43. • Changed register name to M_MEMORY from M_MEMORY0. See Section 17.17 and Table 15. • Added Section 18.3. • Corrected links in Section 18.4, Section 18.5, and Section 18.6. • Corrected links in Section 18.8, Section 18.9, Section 18.10, and Section 18.13. • Removed the following registers from the Section 18 section: – FS_I_NOT_OVUV_SAFE_REACTION1 – FS_I_NOT_OVUV_SAFE_REACTION2 – FS_I_NOT_OVUV_SAFE_REACTION3 – FS_I_NOT_VMON_ABIST2 – FS_I_NOT_WD_CONFIG – FS_I_NOT_SAFE_INPUTS – FS_I_NOT_FSSM – FS_I_NOT_SVS1 – FS_I_NOT_SVS2 – FS_I_NOT_WD_WINDOW • Adjusted footnotes in Section 19.1. • In Section 19.2, Table 99, added frequencies to the Minimum ON Time section and deleted the row for Value 00 in that section. • In Section 19.4, corrected links and changed *steps available* to *steps allowed*. • Updated the BOS: Best of supply Section 20.1 • In Section 22.6, updated Figure 14 and Figure 15.			

Table 186. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• In Section 20.2, Table 122, updated the output capacitance. • Updated Figure 11. • Updated Figure 12. • Updated Figure 14. • Updated Figure 15. • Clarified and updated parameters in Section 22.5. • In Section 22.10, updated Figure 19. • Updated Figure 24. • Updated Figure 20. • Updated Figure 27. • Updated Figure 28. • In Section 23.1, corrected register name from DVS_BUCK to BUCK_DVS. • In Section 23.4, corrected register name from DVS_BUCK to BUCK_DVS, changed VSWIN to V_{BUCK_IN}, and changed the description of C_{IN_BUCK} from *Effective input capacitor (close to BUCK_IN pin)* to *Nominal input capacitor (low ESR/ESL, close to BUCK_IN pin)*, • In Section 25.1, changed *LDO1 input supply is external and can be connected to VPRE or BUCK, or another supply inferior to 5.0 V to LDO1 input supply is external and can be connected to VPRE, BUCK, BOOST or another supply limited to 5.0 V*. • In Section 25.3, Table 131, changed *Input capacitor (close to LDO1_IN pin)* to *Nominal input capacitor (close to LDO1_IN pin)* and *Output capacitor (±30%)* to *Effective output capacitor*. Added minimum and maximum values for C_{OUT_LDO1}. • In Section 26.3, Table 132, changed output capacitance values for 150 mA and 400 mA current capabilities. • In Section 21, Table 123, changed *VPRE or BUCK* to *VPRE, BUCK or BOOST*. • In Section 22 updated Figure 11 and Figure 12. • In Section 22.5, changed expression of these parameters: L_{pi} to L_{PI}, C_{pi1} to C_{PI1}, and Q_g to $Q_{G(tot)}$. Changed *switching frequency on the battery line* to *switching frequency F_{PRE_SW} on the battery line*. • In Section 22.10, updated Figure 19, removed figure titled *Battery switch protection schemes comparison*, and updated the last two paragraphs.			

Table 186. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• Updated Figure 29. • Updated Figure 31. • Updated Figure 32. • Under Section 28, in Section 28.2, updated Figure 32. • Updated Figure 33. • In Section 30.2, changed title of table. Changed table column heading from *Phase delay code ph[2:0]* to *Phase delay code PH[2:0]*. Changed *000* to *000 (default)* and *no delay (default)* to *no delay*. • In Section 30.4.2, changed the last word from *content* to *spreading*. • In Section 31.1, updated Figure 35. • In Section 31.3, exchanged the order of this List item and this List item. • In Section 31.4, inserted words *first* and *then in* to get this sentence: *The watchdog configuration must be written first in the FS_WD_WINDOW_DUR and then in the FS_NOT_WD_WINDOW_DUR registers like INIT registers.* • In Section 31.4, updated Figure 36. • Updated Figure 37. • Updated Section 31.4.2, including table heading and format. • Updated Figure 39. • In Section 31.6.8, Table 169, added *default* after 000 in the first column and replaced *default* in the second column with *flag only if OV*. Also in the second column, replaced *PWRDWN_DFS (D-FS if OV)* with *PWRDWN_DFS (DEEP-FS if OV)*. • In Section 31.8.1, updated Figure 45 and Figure 46. • Updated Table 177. • In Section 32, updated Figure 50. • Moved this section Section 15 about I^2C up to just after the *Functional description* section.			
FS8600 v.1	20211115	Product	—	—
Modifications:	• Initial Release			

35 Legal information

35.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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